



DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

At. Po. Lonere, Tal. Mangaon, Dist. Raigad 402 103 MS (www.dbatuonline.com)

INVITATION FOR QUOTATION

08 OCT 2026

Our Ref No. : DBATU/Store/EXTC Dept/Cadency Software / 2026-27/ 4478

Date: 8/10/2026

Quotation For: Cadency Software (20 Users)

Due On: 21/10/2026

Date of Opening: 22/10/2026

Time: 11:00 am

To,

Sub: QUOTATION FOR THE SUPPLY OF STORE

Dear Sir,

Your quotation for the items listed overleaf, may please be submitted to the under signed, so as to reach this Office not later than: 21/10/2026.

While submitting your quotation, the following procedure may please be observed and other points borne in mind.

01. The maker's name must be specified.
02. The "Terms and Conditions" for supply and delivery of stores, should be clearly indicated in the quotation, stating whether rates are, inclusive of all taxes, Packing and forwarding charges Freight charges, etc. or not, however rates offered as including all taxes will be more welcome.
03. If packing and forwarding charges are to be charged separately, it should be so clearly stated in your quotation.
04. Please mention clearly whether consignment would be Ex-Godown, Ex-Shop, of F.O.R. dispatching stations. Preferably terms offered as "Delivery of consignment of stores, on F.O.R.
05. Envelope should be clearly marked with our reference No and date of this quotation. It should also be superscripted as per the format given above.
06. The quotation would be opened as per date and timing given above, if desired by you, you may depute an authorized representative with a letter of authority to be present at the time of opening of the quotation at this Office on the aforesaid day, date & time.
07. Your quotation must be valid for a minimum 30 (Thirty) working days from the date of its opening.
08. Quotation received after the date of opening may not be taken into consideration.
09. Items tendered should confirm to the specification shown in the attached list when and where, full or no specifications are indicated against items in the list. Kindly furnish your full specification in accordance with accepted standards against each item tendered. Where reference to catalogue is made, the relevant catalogues/ Pamphlets/ Literature should accompany the quotation.
10. Your quotation should be for all new items and not for second hand.
11. Please state whether items will be available Ex-Stock. If not the minimum period for delivery, or for supplying the items or stores.
12. It should be clearly stated whether **GST**, Insurance, Freight or packing and forwarding charges, or any other taxes and duties, etc. leviable.
13. It would be appreciated if illustrated catalogues/Literature etc is furnished with the quotation.



14. Expression to as "Complete with standard Equipment" complete with standard accessories "Equipment to" As good as should be avoided. If at all their use is unavoidable then it should be very specifically indicated as to what exactly they mean and what exactly would be supplied under them. Any ambiguity or vagueness should be avoided.
15. For convenience, kindly adopt while quoting the same serial Nos. as given in the list detailed below.
16. Special Terms: Following terms and condition are also required

Type of item-proprietary nature software

I. Original equipment manufacturer (OEM) or its authorized dealer only can participate.

II. If the participant is the dealer then OEM authorization certificate is required.

III. Demonstration with training must be provide to our staff, faculty and students at our premises at the offline or online mode.

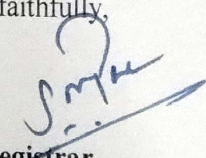
IV. You would provide free of cost all the backup support and upgrades of the software for a period of license usage (5 Year) without additional any cost.

V. You would submit a certificate from Head of Department about supply and installation of the software on the departmental computers along with Software Material /Soft Copies containing user's manual for software, If possible

VI. All the required document should submit with the seal and signature of the concern authority.

VII. Tender fee Rs. 3000/- and EMD Rs. 50,000/-
Thanking You.

Yours faithfully,


Registrar

Dr. Babasaheb Ambedkar Technological University,
Lonere

List of Items

Sr. No.	Description	Make	Qty.	Rate	Amount
01	Cadency Software (20 Users) (Details Specification are as per over Leaf)		01		

* Quantity may vary

Specifications for Cadence Level 1 Bundle

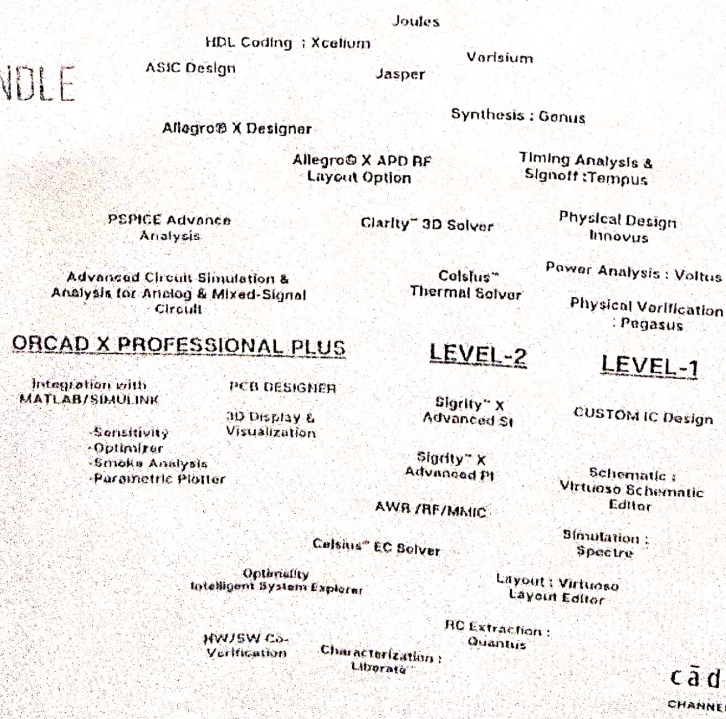
Microwave Office Commercial & Academic Evaluation feature set	Virtuoso® MultiTech Framework
Conformal™ GXL	Virtuoso® Schematic Editor XL
Conformal® Low Power XL	Virtuoso® Power Manager
Conformal® Low Power GXL	Virtuoso® ADE Explorer
Conformal® ECO Designer GXL	Virtuoso® Visualization & Analysis XL
Virtuoso® Digital Implementation	Virtuoso® ADE Assembler
Genus™ Low Power Option	Virtuoso® Variation Option
Genus™ Physical Option	Virtuoso® ADE Simulation Manager
Genus™ CPU Accelerator Option	Virtuoso® ADE Verifier
Genus™ Synthesis Solution	Virtuoso® DFM Interactive
Innovus™ 3nm Option	Virtuoso® Layout Suite GXL
Innovus™ 7nm Option	Virtuoso® Implementation Aware Design Option
Innovus™ 20/16/14nm Option	Virtuoso® Advanced Node Option for Layout
Innovus™ Mixed Signal Option	Virtuoso® Advanced Node Option for Layout Standard
Innovus™ High Frequency Route Option	Cadence® iPegasus™ DRC for Virtuoso Studio
Innovus™ Hierarchical Design Option	Cadence® iPegasus™ FILL for Virtuoso Studio
Innovus™ GigaPlace XL Option	Virtuoso® Photonics Option
Innovus™ GigaPlace-GXL Option	Virtuoso® Layout Suite EAD
Innovus™ Power Integrity Option	Virtuoso® RF Platform
Innovus™ Automotive Flow Option	Virtuoso® Layout Suite EXL
Innovus™ CPU Accelerator Option	Virtuoso® Layout Suite MXL
Innovus™ Implementation System	Voltus™-XFI Custom Power Integrity Solution
Joules™ Implementation Option	Verifault XL Simulator
Joules™ Multihost Option	Verifault XL Slave Node License
Joules™ RTL Power Solution XL	Jasper™ RTL Designer Apps Option
EMX™ Planar 3D Solver SYSS00	Jasper™ Lint & DFT Designer App
Helium™ Creation and SW Development Environment	Jasper™ Formal Apps Option
Cadence® Framework Integration Runtime Option	Jasper™ Advanced Platform Option
Virtuoso® Simulation Environment	Jasper™ Formal Verification Platform
Virtuoso® Schematic Editor HSPICE Interface	Jasper™ Coverage Unreachability APP
Cadence® SKILL Development Environment	Jasper™ Verification Apps Option
Virtuoso® EDIF 200 Reader	Liberate™ Trio ALT910
Virtuoso® EDIF 200 Writer	Conformal® Litmus Signoff
Cadence® Design Framework Integrator's Toolkit	Conformal® Litmus Constraint Management Option
Virtuoso® Schematic VHDL Interface	Midas™ Safety Platform
Virtuoso® Schematic Editor Verilog® Interface	Medus ATPG – Distributed CPU Option
Virtuoso® Analog Oasis Run-Time Option	Modus DFT Option
Cadence® OASIS for RFDE	Modus Hierarchical Option
Virtuoso® Analog HSPICE Interface Option	Modus ATPG – Distributed Base
Virtuoso® AMS Designer Environment	Error Cell Generator
Virtuoso® Advanced Node Framework	Graphical Technology Editor
Allegro® X SIP Layout Bundle	Pcell Generator
Spectre® Characterization Simulator Option	Cadence® Pegasus™ 16nm Node
Cadence® SimVision Mixed-Signal Debug Option	Cadence® Pegasus™ Design Rule Check
Spectre® RelXpert Reliability Simulator	Cadence® Pegasus™ Layout vs. Schematic Check
Cadence® Pegasus™ DFM Fill	Interactive mode for Spectre® using Python/TCL
Cadence® Pegasus™ Results Viewer	Spectre® AMS Designer
Cadence® Pegasus™ Programmable Electrical Rule Check	Spectre® MMSIM with Spectre X Simulator
Cadence® Pegasus™ Design Review	Spectre® Power Option
Cadence® Pegasus™ Custom Fill	Spectre® CPU Accelerator Option
Cadence® Pegasus™ User Interface	Tempus™ Timing Signoff Solution L
Cadence® Pegasus™ Design Review Layout and Mask Data Viewer	Tempus™ Timing Signoff Solution XL
Innovus™ DFM Option INVSS0	Tempus™ Advanced Analysis Option
Pegasus™ Layout Pattern Analyzer	Tempus™ Timing Signoff Solution ECO
	Tempus™ Timing Signoff Solution MP

Pegasus™ Layout Pattern Fixing Option
 Cadence® Quantus™ Extraction XL
 Cadence® Quantus™ Advanced Analysis GXL Option
 Cadence® Quantus™ Advanced Modeling GXL Option
 Cadence® Quantus™ Display Technology Option
 Cadence® Quantus™ Advanced Modeling20 GXL Option
 Cadence® Quantus™ Advanced Node Modeling Option
 Quantus™ 32/28nm to 10nm Option
 Cadence® Quantus™ 7nm Option
 Sigrity™ X Aurora PCB Analysis
 Sigrity™ X PowerSI
 Sigrity™ X SPEEDEM
 Sigrity™ X Advanced SI
 Sigrity™ X Advanced PI
 Sigrity™ X SystemsPI Option
 Sigrity™ X Advanced IBIS Modeling
 Allegro® X Designer
 Allegro® X Venture
 Allegro® Design Publisher XL
 Allegro® X Productivity Toolbox
 Allegro® PCB Symphony Team Design Option
 Allegro® Library Authoring
 OrCAD® X Professional Plus
 Pspice® System Designer
 Allegro® X Silicon Layout Option
 Allegro® X APD RF Layout Option
 Integrity® System Planner

Tempus™ Power Integrity Option
 Voltus™ IC Power Integrity Solution XL
 Voltus™ IC Power Integrity Solution GXL Option
 Voltus™ IC Power Integrity Solution
 Voltus™ 3DIC Power Integrity Option
 Voltus™ IC Power Integrity Solution
 Stratus™ HLS XL
 Celsius™ Thermal Solver
 Celsius™ Studio Advanced
 Clarity™ 3D Solver
 Multi-Physics Universal HPC Accelerator
 Clarity™ 3D Transient Solver
 Clarity™ PCB Extraction Suite
 Clarity™ IC Package Extraction Suite
 Clarity™ Advanced IC Package Extraction
 Optimality™ Explorer Essentials
 Celsius™ Advanced PTI
 Celsius™ EC Solver
 Indago™ Embedded Software Debug App
 Verisium™ Debug for Simulation
 vManager™ Safety
 vManager™ Linux Client (Quantity 5)
 vManager™ Project Server
 Enterprise Simulator XL Interface for MTI 29661
 Enterprise Simulator XL Interface for VCS 29671
 Xcelium™ Digital Mixed Signal App
 Xcelium™ Single Core
 Xcelium™ Digital Mixed Signal Option
 Xcelium™ Safety Simulation

CADENCE

ASIC DESIGN BUNDLE



AGENDA FOR POST INSTALLATION TRAINING

Day 1

FULL CUSTOM DESIGN FLOW

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Symbol Creation
- Testbench Creation using Virtuoso Schematic Editor
- Functional Simulation using Spectre
- Layout Design using Virtuoso Layout Editor
- Physical Verification which includes DRC & LVS
- Parasitic Extraction using Quantus
- Post Layout Simulation
- Generation of GDSII

Note:

- The entire Full Custom IC Design Flow will be demonstrated by considering CMOS Inverter as an example.
- 1-day Training for new customers.
- The same case study will be demonstrated for renewal orders as a half-day session.

Day 2SEMI-CUSTOM DESIGN FLOW

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution
- DFT (Design for Testability) using Modus
- LEC (Logical Equivalence Check) using Conformal
- Physical Implementation using Innovus that includes
 - ✓ Floor Planning
 - ✓ Power Planning
 - ✓ Placement
 - ✓ CTS
 - ✓ Routing
- Timing Analysis using Tempus
- Power Analysis using Voltus
- Parasitic Extraction
- Generation of GDSII

Note:

- The entire Semi-Custom IC Design Flow will be demonstrated by considering 8-bit Counter as an example.
- 1-day Training for new customers.
- The same case study will be demonstrated for renewal orders as a half-day session.