

**Dr. Babasaheb Ambedkar Technological University (Established a University of
Technology in the State of Maharashtra)
(Under Maharashtra Act No. XXIX of 2014)**

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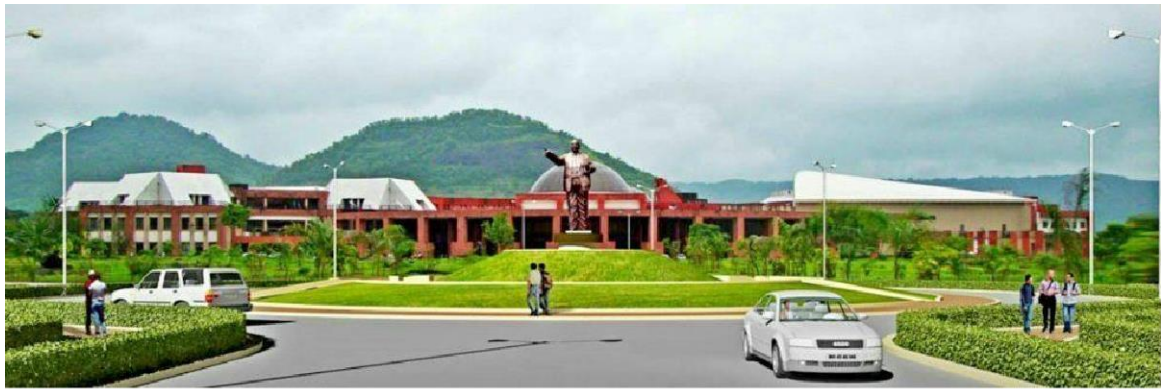
CURRICULUM OF UNDERGRADUATE PROGRAMME B. TECH

Electronics Engineering (VLSI Design and Technology)

Second Year [2024-25]

Third Year [2025-26]

Final Year [2026-27] and onwards



With effective from academic year 2024-25

Rules and Regulations

The normal duration of the course leading to B. Tech degree will be EIGHT semesters.

The normal duration of the course leading to M. Tech. degree will be FOUR semesters.

Each academic year shall be divided into 2 semesters, each of 20 weeks duration, including evaluation and grade finalization, etc. The Academic Session in each semester shall provide for at least 90 Teaching Days, with at least 40 hours of teaching contact periods in a five to six days session per week. The semester that is typically from Mid-July to November is called the ODD SEMESTER, and the one that is from January to Mid-May is called the EVEN SEMESTER. Academic Session may be scheduled for the Summer Session/Semester as well. For 1st year B. Tech and M. Tech the schedule will be decided as per the admission schedule declared by Government of Maharashtra.

The schedule of academic activities for a Semester, including the dates of registration, mid-semester examination, end- semester examination, inter-semester vacation, etc. shall be referred to as the Academic Calendar of the Semester, which shall be prepared by the Dean (Academic), and announced at least TWO weeks before the Closing Date of the previous Semester.

The Academic Calendar must be strictly adhered to, and all other activities including co-curricular and/or extra -curricular activities must be scheduled so as not to interfere with the Curricular Activities as stipulated in the Academic Calendar.

REGISTRATION:

1. Lower and Upper Limits for Course Credits Registered in a Semester, by a Full-Time Student of a UG/PG Programme: A full time student of a particular UG/PG programme shall register for the appropriate number of course credits in each semester/session that is within the minimum and maximum limits specific to that UG/PG programme as stipulated in the specific Regulations pertaining to that UG/PG programme.
2. Mandatory Pre-Registration for higher semesters: In order to facilitate proper planning of the academic activities of a semester, it is essential for the every institute to inform to Dean (Academics) and COE regarding details of total no. of electives offered (Course-wise) along with the number of students opted for the same. This information should be submitted within two weeks from the date of commencement of the semester as per academic calendar.
3. PhD students can register for any of PG/PhD courses and the corresponding rules of evaluation will apply.
4. Under Graduate students may be permitted to register for a few selected Post Graduate courses, in exceptionally rare circumstances, only if the DUGC/DPGC is convinced of the level of the academic achievement and the potential in a student.

Course Pre-Requisites:

1. In order to register for some courses, it may be required either to have exposure in, or to have completed satisfactorily, or to have prior earned credits in, some specified courses.
2. Students who do not register on the day announced for the purpose may be permitted LATE REGISTRATION up to the notified day in academic calendar on payment of late fee.

3. REGISTRATION IN ABSENTIA will be allowed only in exceptional cases with the approval of the Dean (Academic) / Principal.

4. A student will be permitted to register in the next semester only if he fulfills the following conditions:

- (a) Satisfied all the Academic Requirements to continue with the programme of Studies without termination
- (b) Cleared all Institute, Hostel and Library dues and fines (if any) of the previous semesters;
- (c) Paid all required advance payments of the Institute and hostel for the current semester;
- (d) Not been debarred from registering on any specific ground by the Institute.

EVALUATION SYSTEM:

1. Absolute grading system based on absolute marks as indicated below will be implemented from academic year 2020-21, starting from I year B. Tech.

Percentage of Marks	Letter Grade	Grade Point
91-100	EX	10.0
86-90	AA	9.0
81-85	AB	8.5
76-80	BB	8.0
71-75	BC	7.5
66-70	CC	7.0
61-65	CD	6.5
56-60	DD	6.0
51-55	DE	5.5
40-50	EE	5.0
<40	EF	0.0

2. Class is awarded based on CGPA of all eight semesters of B. Tech Program.

CGPA for pass is minimum 5.0	
CGPA up to < 5.50	Pass class
CGPA $\geq$ 5.50 & < 6.00	Second Class
CGPA $\geq$ 6.00 & < 7.50	First Class
CGPA $\geq$ 7.50	Distinction
[Percentage of Marks =CGPA*10.0]	

3. A total of 100 Marks for each theory course is distributed as follows:

1	Mid Semester Exam (MSE) Marks	20
2	Continuous Assessment Marks	20
3	End Semester Examination (ESE) Marks	60

4. A total of 100 Marks for each practical course is distributed as follows:

1.	Continuous Assessment Marks	60
2.	End Semester Examination (ESE)Marks	40

It is mandatory for every student of B. Tech to score a minimum of 40 marks out of 100, with a minimum of 20 marks out of 60 marks in End Semester Examination for theory course.

This will be implemented from the first year of B. Tech starting from Academic Year 2023-24.

5. Description of Grades:

EX Grade: An “EX” grade stands for outstanding achievement.

Grade: The “EE” grade stands for minimum passing grade.

The students may appear for the remedial examination for the subjects he/she failed for the current semester of admission only and his/her performance will be awarded with EE grade only. If any of the student remain absent for the regular examination due to genuine reason and the same will be verified and tested by the Dean (Academics) or committee constituted by the University Authority.

Grade: The “FF” grade denotes very poor performance, i.e. failure in a course due to poor performance. The students who have been awarded “FF” grade in a course in any semester must repeat the subject in next semester.

1. Evaluation of Performance:

1.1. Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA)

(A) Semester Grade Point Average (SGPA) The performance of a student in a semester is indicated by Semester Grade Point Average (SGPA) which is a weighted average of the grade points obtained in all the courses taken by the student in the semester and scaled to a maximum of 10. (SGPI is to be calculated up to two decimal places). A Semester Grade Point Average (SGPA) will be computed for each semester as follows:

$$SGPA = \frac{[\sum_{i=1}^n c_i g_i]}{[\sum_{i=1}^n c_i]}$$

Where

“n” is the number of subjects for the semester,

“ci” is the number of credits allotted to a particular subject, and

“gi” is the grade-points awarded to the student for the subject based on his performance as per the above table.

-SGPA will be rounded off to the second place of decimal and recorded as such.

(B) Cumulative Grade Point Average (CGPA): An up to date assessment of the overall performance of a student from the time he entered the Institute is obtained by calculating Cumulative Grade Point Average (CGPA) of a student. The CGPA is weighted average of the grade points obtained in all the courses registered by the student since he/she

entered the Institute. CGPA is also calculated at the end of every semester (upto two decimal places). Starting from the first semester at the end of each semester (S), a Cumulative Grade Point Average (CGPA) will be computed as follows:

$$CGPA = \frac{[\sum_{i=1}^m c_i g_i]}{[\sum_{i=1}^m c_i]}$$

Where

“m” is the total number of subjects from the first semester onwards up to and including the semester S,

“ci” is the number of credits allotted to a particular subject, and

“gi” is the grade-points awarded to the student for the subject based on his/her performance as per the above table.

#CGPA will be rounded off to the second place of decimal and recorded as such.

Awwads of Degree of Honours Major Degree

The concept of Major and Minors at B. Tech level is introduced to enhance learning skills of students, acquisition of additional knowledge in domains other than the discipline being pursued by the student, to make the students better employable with additional knowledge and encourage students to pursue cross-discipline research.

A. Eligibility Criteria for Majors

1. The Student should have Minimum CGPA of 7.5 up to 4th Semester
2. Student willing to opt for majors has to register at the beginning of 5th Semester
3. The Student has to complete 5 additional advanced courses from the same discipline specified in the curriculum. These five courses should be of 4 credits each amounting to 20 credits. The students should complete these credits before the end of last semester.
4. Student may opt for the courses from NPTEL/ SWAYAM platform. (if the credits of NPTEL/ SWAYAM courses do not match with the existing subject proper scaling will be done)

Student complying with these criteria will be awarded B. Tech (Honors) Degree.

B. Eligibility Criteria for Minors

1. The student should have Minimum CGPA of 7.5 up to 4th Semester
2. Student willing to opt for minors has to register at the beginning of 5th Semester
3. The student has to complete 5 additional courses from other discipline of their interest, which are specified in the respective discipline. These five courses should be of 4 credits each amounting to 20 credits.
4. Student may opt for the courses from NPTEL/ SWAYAM platform. (if the credits of NPTEL/ SWAYAM courses do not match with the existing subject proper scaling will be done)

Student complying with these criteria will be awarded with B. Tech Degree in Engineering with Minor in -----Engineering
(For e.g.: B. Tech in Electronics Engineering (VLSI Design and Technology) with Minor in Computer Engineering).

For applying for Honors and Minor Degree the student has to register themselves through the proper system.

ATTENDANCE REQUIREMENTS:

1. All students must attend every lecture, tutorial and practical classes.
2. To account for approved leave of absence (e.g. representing the Institute in sports, games or athletics; placement activities; NCC/NSS activities; etc.) and/or any other such contingencies like Medical emergencies, etc., the attendance requirement shall be a minimum of 75% of the classes actually conducted.
 - a) If the student failed to maintain 75% attendance, he/she will be detained for appearing the successive examination.
 - b) The Dean (Academics)/ Principal is permitted to give 10% concession for the genuine reasons as such the case may be.
 - c) In any case the student will not be permitted for appearing the examination if the attendance is less than 65%.
3. The course instructor handling a course must finalize the attendance 3 calendar days before the last day of classes in the current semester and communicate clearly to the students by displaying prominently in the department and also in report writing to the head of the department concerned.
4. The attendance records are to be maintained by the course instructor and he shall show it to the student, if and when required.

TRANSFER OF CREDITS

The courses credited elsewhere, in Indian or foreign University/Institutions/ Colleges/ Swayam Courses by students during their study period at DBATU may count towards the credit requirements for the award of degree. The guidelines for such transfer of credits are as follows:

- a) 20 % of the total credit will be considered for respective calculations.
- b) Credits transferred will be considered for overall credits requirements of the programme.
- c) Credits transfer can be considered only for the course at same level i. e UG, PG etc.
- d) A student must provide all details (original or attested authentic copies) such as course contents, number of contact hours, course instructor /project guide and evaluation system for the course for which he is requesting a credits transfer. He shall also provide the approval or acceptance letter from the other side. These details will be evaluated by the concerned Board of Studies before giving approval. The Board of Studies will then decide the number of equivalent credits the student will get for such course(s) in DBATU. The complete details will then be forwarded to Dean for approval.
- e) A student has to get minimum passing grades/ marks for such courses for which the credits transfers are to be made.
- f) Credits transfers availed by a student shall be properly recorded on academic record(s) of the student.
- g) In exceptional cases, the students may opt for higher credits than the prescribed.

B. Tech. in Electronics Engineering (VLSI Design and Technology)
Different Categories of Courses and Credits for Degree Requirements

a) Humanities and Social Science including Management Courses

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV403	Basic Human Rights	(3-0-0) 3
2	BTEEV505	A. Economics and Management B. Business Communication C. Profession Ethics and Values D. Project Management	(3-0-0) 3
3	BTEEV605	A. Development Engineering B. Employability and Skills Development C. Consumer Behavior	(3-0-0) 3
4	BTEEV706	A. Foreign Language Studies B. Universal Human Values and Ethics C. Intellectual Property Rights	(1-1-0) Audit
TOTAL			9

b) Basic Science Course

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV301	Engineering Mathematics – III	(3-1-0) 4
2	BTEEV404	Probability Theory and Random Processes	(3-0-0) 3
TOTAL			07

c) Engineering Science Course

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV304	Network Theory & Signal and System	(3-1-0) 4
2	BTEEV305	Python Programming	(3-0-0) 3
3	BTEEV308	Python Programming Lab	(0-0-2) 1
TOTAL			08

d) Professional Core Course

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV302	Electronic Devices & Circuits	(3-0-0) 3
2	BTEEV303	Digital Electronics & Microprocessor	(3-1-0) 4
3	BTEEV401	Digital System Design using HDL	(3-1-0) 4
4	BTEEV402	Analog Circuits	(3-1-0) 4
5	BTEEV501	Introduction to VLSI Life Cycle & Micro-fabrication	(3-0-0) 3
6	BTEEV502	Microcontroller & Embedded System	(3-1-0) 4
7	BTEEV601	Internet of Things & Industry 4.0	(3-1-0) 4
8	BTEEV602	Digital VLSI Design	(3-0-0) 3
9	BTEEV701	Digital Signal Processing	(3-0-0) 3
10	BTEEV702	Analog VLSI Design	(3-0-0) 3
11	BTEEV703	VLSI Verification & Testing	(3-0-0) 3
12	BTEEV306	EDC Lab	(0-0-2) 1

13	BTEEV307	Digital Electronics & Microprocessor Lab	(0-0-2) 1
14	BTEEV406	Analog Circuits Lab	(0-0-2) 1
15	BTEEV407	Digital System Design using HDL Lab	(0-0-2) 1
16	BTEEV506	Introduction to VLSI Life Cycle Lab	(0-0-2) 1
17	BTEEV507	Microcontroller & Embedded System Lab	(0-0-2) 1
18	BTEEV606	Digital VLSI Lab	(0-0-2) 1
19	BTEEV707	Digital Signal Processing Lab	(0-0-2) 1
20	BTEEV708	VLSI Verification & Testing Lab	(0-0-2) 1
21	BTEEV709	Analog VLSI Design Lab	(0-0-2) 1
TOTAL			48

e) Professional Elective Course

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV405	Professional Elective Courses –I A. Analog and Digital Communication B. Electrical Measurement & Instrumentation C. Data Structure & Algorithms using C++ D. Sensors & Actuators	(3-0-0) 3
2	BTEEV408	3. Professional Elective Courses –I Lab A. Analog and Digital Communication B. Electrical Measurement & Instrumentation C. Data Structure & Algorithms using C++ D. Sensors & Actuators	(0-0-2) 1
3	BTEEV503	Professional Elective Course (PEC) -II A. Control System Engineering B. Electromagnetic Field Theory C. High Speed Devices & Circuits D. Semiconductor Device Modeling	(3-1-0) 4
4	BTEEV603	Professional Elective Course (PEC) -III A. Power Electronics & Drives B. Semiconductor Materials Synthesis & Characterization C. Computer Networks D. Introduction to MEMS	(3-1-0) 4
5	BTEEV607	Professional Elective Course (PEC) –III Lab A. Power Electronics & Drives B. Semiconductor Materials Synthesis and Characterization C. Computer Networks D. Introduction to MEMS	(0-0-2) 1
6	BTEEV704	Professional Elective Course (PEC) -IV A. Low Power VLSI Design B. Semiconductor Packaging and Testing C. System on Chip D. Quantum Computing	(3-1-0) 4
TOTAL			17

f) Open Elective Course

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV504	Open Elective Course (OEC) - I A. Java Programming B. Database Management Systems C. Software Engineering D. Robotics and Automation	(3-0-0) 3
2	BTEEV508	3. Open Elective Course (OEC) – I Lab A. Java Programming B. Database Management Systems C. Software Engineering D. Robotics and Automation	(0-0-2) 1
3	BTEEV604	Open Elective Course (OEC) - II A. Artificial Intelligence & Machine Learning B. Android Programming C. Cloud Computing D. PLC & Automation	(3-0-0) 3
4	BTEEV608	Open Elective Course (OEC) – II Lab A. Artificial Intelligence & Machine Learning B. Android Programming C. Cloud Computing D. PLC & Automation	(0-0-2) 1
5	BTEEV705	Open Elective Course (OEC) -III A. Deep Learning & Data Science B. Linux OS C. Cyber Security D. Advanced Communication Technology	(3-1-0) 4
TOTAL			12

g) Seminar / Mini Project / Internship

Sr. No.	Course Code	Course Name	(L-T-P) Credits
1	BTEEV309	Seminar-I	(0-0-4) 2
2	BTEEV310	Internship –I (Evaluation) / MOOC	Audit
3	BTEEV409	Seminar - II	(0-0-4) 2
4	BTEEV410	Internship –II / MOOC	Audit
5	BTEEV509	Mini Project I	(0-0-4) 2
6	BTEEV510	Internship –II (Evaluation) / MOOC	Audit
7	BTEEV609	Mini Project II	(0-0-4) 2
8	BTEEV610	Internship –III / MOOC	Audit
9	BTEEV710	Project Work	(0-0-4) 2
10	BTEEV711	Internship –IV (Evaluation) / MOOC	Audit
11	BTEEV801	Project Work/ Internship	(0-0-24) 12
TOTAL			22

Category – wise total number of credits

Sr. No	Category	Suggested Breakup of Credits by AICTE	Credits awarded to First year	Credits awarded to Second year to Final Year	Total
1	Humanities and Social Sciences including Management courses	12*	3	9	12
2	Basic Science courses	25*	18	7	25
3	Engineering Science courses including workshop, drawing, basics of electrical / mechanical / computer etc.	24*	15	8	23
4	Professional core courses	48*	0	49	49
5	Professional Elective courses relevant to chosen specialization/branch	18*	0	16	16
6	Open subjects – Electives from other technical and /or emerging subjects	18*	0	12	12
7	Project work, seminar and internship in industry or elsewhere	15*	1	22	23
8	Mandatory Courses [Environmental Sciences, Induction training, Indian Constitution, Essence of Indian Knowledge Tradition]	NC	--	--	--
	Total	160*	37	123	160

**Minor variation is allowed as per need of the respective disciplines.*

Suggested Plan of Study

Number of Courses	Semester							
	I	II	III	IV	V	VI	VII	VIII
1	BTBS101	BTBS201	BTEEV301	BTEEV401	BTEEV501	BTEEV601	BTEEV701	BTEEV801
2	BTBS102	BTBS202	BTEEV302	BTEEV402	BTEEV502	BTEEV602	BTEEV702	--
3	BTES103	BTES203	BTEEV303	BTEEV403	BTEEV503 (PEC-II Elective)	BTEEV603 (PEC-III Elective)	BTEEV703	--
4	BTHM104	BTES204	BTEEV304	BTEEV404	BTEEV504 (OEC -I Elective)	BTEEV604 (OEC -II Elective)	BTEEV704 (PEC-IV Elective)	--
5	BTES105	BTES205	BTEEV305	BTEEV405 (PEC-I Elective)	BTEEV505 (HSSMEC-IV Elective)	BTEEV605 (HSSMEC-V Elective)	BTEEV705 (OEC -III Elective)	--
6	BTES106	BTES206	BTEEV306	BTEEV406	BTEEV506	BTEEV606	BTEEV706 (HSSMEC-VI Elective)	--
7	BTBS107L	BTBS207L	BTEEV307	BTEEV407	BTEEV507	BTEEV607	BTEEV707	--
8	BTES108L	BTES208L	BTEEV308(Internship –I Evaluation)	BTEEV408 (Internship–II)	BTEEV508 (Internship –II Evaluation)	BTEEV608 (Internship–III)	BTEEV708	--
9	BTHM109L	BTES209S					BTEEV709	--
10	--	BTES211P (Internship-I)					BTEEV710 (Project)	--
11							BTEEV711 (Internship–IV Evaluation) / MOOC	

Programme Educational Objectives (PEO)

Name of Programme: B.Tech. Electronics Engineering (VLSI Design and Technology). A graduate in the discipline of VLSI Design and Technology is generally expected to have three kinds of knowledge. First, the graduate should have conceptual knowledge of the core topics of B.Tech. Electronics Engineering (VLSI Design and Technology). Second, she/he should have knowledge of mathematical formalism underlying various programming concepts. Third, graduates in the discipline of B.Tech. Electronics Engineering (VLSI Design and Technology) should have the knowledge of the state of the latest tools and technologies, so that he/she can apply the principles of Electronics Engineering to solve real-life problems from diverse application domains. The programme of B.Tech. Electronics Engineering (VLSI Design and Technology) at Dr. Babasaheb Ambedkar Technological University (DBATU) essentially aims to meet these broad expectations. At the same time, the program intends to comply with the courses and syllabus available at National Program on Technology Enhanced Learning (NPTEL) and SWAYAM. The following specific educational objective aims to achieve these global and regional expectations.

Objective Identifier	Objectives
PEO1	Graduates will be able to apply the fundamental concepts of electronics engineering for electronic system design.
PEO2	Graduates will pursue career in VLSI design and allied fields on cutting edge technologies.
PEO3	Graduates will exhibit professional ethics and teamwork in their profession through lifelong learning.

Programme Outcomes (PO)

After undergoing the learning process of four years, students of B.Tech. Electronics Engineering(VLSI Design and Technology) at Dr. Babasaheb Ambedkar Technological University will have an ability to build information systems and provide computer-based solutions to real life problems. The graduates of this programme will demonstrate following abilities and skill sets.

Outcome Identifier	Outcomes
PO1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

Outcome Identifier	Outcomes
PSO1	Apply knowledge of mathematics and science to solve advanced engineering problems in the areas of micro-electronic devices & circuits, Signal Processing and computation to pursue higher studies.
PSO2	Accomplish advanced practical exposure in the domain of Electronics, IoT and VLSI using contemporary tools and / or equipment's to acquire professional competencies to meet industry standards.

Graduate Attributes / ABET's Criteria

The Graduate Attributes are the knowledge skills and attitudes which the students have at the time of graduation. These Graduate Attributes identified by National Board of Accreditation are as follows:

- (a) Engineering knowledge: An ability to apply knowledge of mathematics, science and engineering.
- (b) Problem analysis: An ability to design and conduct experiments as well as to analyze and interpret data.
- (c) Design / development of solutions: An ability to design a system, a component, or process, to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
- (d) Individual and team work: An ability to function on multidisciplinary teams.
- (e) Problem Solving: An ability to identify, formulate and solve engineering problems.
- (f) Ethics: An understanding of professional and ethical responsibility.
- (g) Communication: An ability to communicate effectively.
- (h) Environment and sustainability: The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and social context.
- (i) Life-long learning: Recognition of the need for and an ability to engage in life-long learning.
- (j) A knowledge of technology: Acknowledge of contemporary issues, and state of art technology
- (k) Modern tool usage: An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.
- (l) Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply in multidisciplinary environments.

Mapping of Programme Outcomes with Graduate Attributes / ABET's Criteria

	A	B	C	D	E	F	G	H	I	J	K	L
PO1	X									X		
PO2		X			X							
PO3			X		X							
PO4			X		X							
PO5											X	
PO6					X					X		
PO7								X				
PO8						X						
PO9				X								
PO10							X					
PO11												X
PO12									X			

Course Structure for Second Year
B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester III (Term 3)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	BSC	BTEEV301	Engineering Mathematics-III	3	1	-	20	20	60	100	4
2	PCC1	BTEEV302	Electronic Devices & Circuits	3	-	-	20	20	60	100	3
3	PCC2	BTEEV303	Digital Electronics & Microprocessor	3	1	-	20	20	60	100	4
4	ESC11	BTEEV304	Network Theory & Signals and Systems	3	1	-	20	20	60	100	4
5	ESC12	BTEEV305	Python Programming	3	-	-	20	20	60	100	3
6	LC1	BTEEV306	EDC Lab	-	-	2	30	-	20	50	1
7	LC2	BTEEV307	Digital Electronics & Microprocessor Lab	-	-	2	30	-	20	50	1
8	LC3	BTEEV308	Python Programming Lab	-	-	2	30	-	20	50	1
9	Seminar	BTEEV309	Seminar-I	-	-	4	60	-	40	100	2
10	Internship	BTEEV310	Internship –I (Evaluation) / MOOC	-	-	-	-	-	-	-	Audit
Total for Semester III				15	3	10	250	100	400	750	23

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course
 PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory Course
 HSSMC = Humanities and Social Science including Management Courses

Course Structure for Second Year
B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester IV (Term 4)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	PCC3	BTEEV401	Digital System Design using HDL	3	1	-	20	20	60	100	4
2	PCC4	BTEEV402	Analog Circuits	3	1	-	20	20	60	100	4
3	HSSMC3	BTEEV403	Basic Human Rights	3	-	-	20	20	60	100	3
4	BSC8	BTEEV404	Probability Theory and Random Processes	3	-	-	20	20	60	100	3
5	PEC-1	BTEEV405	Professional Elective Courses –I	3	-	-	20	20	60	100	3
		BTEEV405A	Analog and Digital Communication								
		BTEEV405B	Electrical Measurement & Instrumentation								
		BTEEV405C	Data Structure & Algorithms using C++								
		BTEEV405D	Sensors & Actuators								
6	LC4	BTEEV406	Analog Circuits Lab	-	-	2	30	-	20	50	1
7	LC5	BTEEV407	Digital System Design using HDL	-	-	2	30	-	20	50	1
8	LC6	BTEEV408	PEC-1 Lab	-	-	2	30	-	20	50	1
9	Seminar	BTEEV409	Seminar - II	-	-	4	60	-	40	100	2
10	Internship	BTEEV410	Internship –II / MOOC	-	-	-	-	-	-	-	Audit
Total for Semester IV				15	2	10	250	100	400	750	22

Note: The Lab of Professional Elective Courses –I (PEC1) (BTEEV405) should be conducted as per syllabus contents.

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course
 PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory Course
 HSSMC = Humanities and Social Science including Management Courses

Course Structure for Third Year

B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester V (Term 5)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	PCC5	BTEEV501	Introduction to VLSI Life Cycle & Micro-fabrication	3	-	-	20	20	60	100	3
2	PCC6	BTEEV502	Microcontroller & Embedded System	3	1	-	20	20	60	100	4
3	PEC-2	BTEEV503	Professional Elective Course (PEC) -II	3	1	-	20	20	60	100	4
		BTEEV503A	Control System Engineering								
		BTEEV503B	Electromagnetic Field Theory								
		BTEEV503C	High Speed Devices & Circuits								
		BTEEV503D	Semiconductor Device Modeling								
4	OEC-1	BTEEV504	Open Elective Course (OEC) - I	3	-	-	20	20	60	100	3
		BTEEV504A	Java Programming								
		BTEEV504B	Database Management Systems								
		BTEEV504C	Software Engineering								
		BTEEV504D	Robotics								
5	HSSMEC-4	BTEEV505	Humanities and Social Sciences including Management Elective Course - I	3	-	-	20	20	60	100	3
		BTEEV505A	Economics & Management								
		BTEEV505B	Business Communication								
		BTEEV505C	Professional Ethics and Values								
		BTEEV505D	Project Management								
6	LC7	BTEEV506	Introduction to VLSI Life Cycle Lab	-	-	2	30	-	20	50	1
7	LC8	BTEEV507	Microcontroller & Embedded System Lab	-	-	2	30	-	20	50	1
8	LC9	BTEEV508	OEC-1 Lab	-	-	2	30	-	20	50	1
9	PROJ	BTEEV509	Mini Project I	-	-	4	60	-	40	100	2
10	Internship	BTEEV510	Internship –II (Evaluation) / MOOC	-	-	-	-	-	-	-	Audit
Total for Semester V				15	2	10	250	100	400	750	22

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course
 PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory
 Course HSSMC = Humanities and Social Science including Management Courses

Course Structure for Third Year

B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester VI (Term 6)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	PCC7	BTEEV601	Internet of Things & Industry 4.0	3	1	-	20	20	60	100	4
2	PCC8	BTEEV602	Digital VLSI Design	3	-	-	20	20	60	100	3
3	PEC-3	BTEEV603	Professional Elective Course (PEC) -III	3	1	-	20	20	60	100	4
		BTEEV603A	Power Electronics & Drives								
		BTEEV603B	Semiconductor Materials Synthesis and Characterization								
		BTEEV603C	Computer Networks								
		BTEEV603D	Introduction to MEMS								
4	OEC-2	BTEEV604	Open Elective Course (OEC) - I	3	-	-	20	20	60	100	3
		BTEEV604A	Artificial Intelligence & Machine Learning								
		BTEEV604B	Android Programming								
		BTEEV604C	Cloud Computing								
		BTEEV604D	PLC & Automation								
5	HSSMEC - 5	BTEEV605	Humanities and Social Sciences including Management Elective Course (HSSMEC) - II	3	-	-	20	20	60	100	3
		BTEEV605A	Development Engineering								
		BTEEV605B	Employability and Skill Development								
		BTEEV605C	Consumer Behaviour								
6	LC10	BTEEV606	Digital VLSI Design Lab	-	-	2	30	-	20	50	1
7	LC11	BTEEV607	Internet of Things & Industry 4.0 Lab	-	-	2	30	-	20	50	1
8	LC12	BTEEV608	OEC-2 Lab	-	-	2	30	-	20	50	1
9	PROJ	BTEEV609	Mini Project II	-	-	4	60	-	40	100	2
10	Internship	BTEEV610	Internship –III / MOOC	-	-	-	-	-	-	-	Audit
Total for Semester VI				15	2	10	250	100	400	750	22

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory Course HSSMC = Humanities and Social Science including Management Courses

Course Structure for Final Year

B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester VII (Term 7)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	PCC9	BTEEV701	Digital Signal Processing	3	-	-	20	20	60	100	3
2	PCC10	BTEEV702	Analog VLSI Design	3	-	-	20	20	60	100	3
3	PCC11	BTEEV703	VLSI Verification & Testing	3	-	-	20	20	60	100	3
4	PEC-4	BTEEV704	Professional Elective Course (PEC) -IV	3	1	-	20	20	60	100	4
		BTEEV704A	Low Power VLSI Design								
		BTEEV704B	Semiconductor Packaging and Testing								
		BTEEV704C	System on Chip								
		BTEEV704D	Quantum Computing								
5	OEC-3	BTEEV705	Open Elective Course (OEC) - III	3	1	-	20	20	60	100	4
		BTEEV705A	Deep Learning & Data Science								
		BTEEV705B	Linux OS								
		BTEEV705C	Cyber Security								
		BTEEV705D	Advanced Communication Technology								
6	HSSMEC - 6	BTEEV706	Humanities and Social Sciences including Management Elective Course (HSSMEC) - II	1	1	-	-	-	-	-	Audit
		BTEEV706A	Foreign Language Studies								
		BTEEV706B	Universal Human Value & Ethics								
		BTEEV706C	Intellectual Property Rights								
7	LC13	BTEEV707	Digital Signal Processing Lab	-	-	2	30	-	20	50	1
8	LC14	BTEEV708	VLSI Verification & Testing Lab	-	-	2	30	-	20	50	1
9	LC15	BTEEV709	Analog VLSI Design Lab	-	-	2	30	-	20	50	1
10	PROJ	BTEEV710	Project Work	-	-	4	60	-	40	100	2
11	Internship	BTEEV711	Internship –IV (Evaluation)/ MOOC	-	-	-	-	-	-	-	Audit
Total for Semester VII				16	3	10	250	100	400	750	22

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory Course HSSMC = Humanities and Social Science including Management Courses

Course Structure for Final Year

B. Tech in Electronics Engineering (VLSI Design and Technology)

Semester VIII (Term 8)											
Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	Project/ Internship	BTEEV801	Project Work/ Internship	-	-	24	60	-	40	100	12
	Total for Semester VIII			0	0	24	60	-	40	100	12

BSC = Basic Science Course, ESC = Engineering Science Course, PCC = Professional Core Course PEC = Professional Elective Course, OEC = Open Elective Course, LC = Laboratory Course HSSMC = Humanities and Social Science including Management Courses

Final Year (Semester-VII)

Digital Signal Processing

BTEEV701	Digital Signal Processing	PCC-9	3L- 0T - 0P	3 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Introduce fundamental concepts of discrete-time signals and digital signal processing.
2. Develop understanding of Z-transform and its application in system analysis.
3. Explain frequency domain representation using DFT and FFT techniques.
4. Provide knowledge of digital filter design methods for IIR filters.
5. Enable design and realization of FIR filters for signal processing applications.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain discrete-time signals, sampling concepts, and basic principles of digital signal processing.
CO2	Apply Z-transform techniques to analyze systems and solve difference equations.
CO3	Convert signals in frequency domain using DFT and FFT algorithms.
CO4	Design and implement FIR & IIR filters using standard methods and realizations.
CO5	Illustrate application of DSP in Multirate signal processing context.

Course Contents:

Unit 1: Fundamental of DSP

[8 hours]

Sampling and reconstruction of signals, Discrete time signals, representation of DT signals, operations on DT Signals, Basic elements of DSP, advantages of DSP over ASP, Classification of Discrete Time Signals, Classification of Discrete Time Systems, LTI Systems, Convolution.

Unit 2: Z transform

[7 hours]

Need for transform, Definition & Properties of Z-Transform, ROC & its properties, System Stability in Z-domain, Inverse Z transform: Power series method, Partial Fraction Expansion method, Solution of difference equations.

Unit 3: Discrete Fourier Transform

[8 Hours]

DTFT: Definition & Properties, Frequency domain sampling.

DFT: Properties, circular convolution, Computation of linear convolution using DFT, IDFT

FFT: Decimation in time and Decimation in frequency using Radix-2 FFT algorithm.

Unit 4: Digital Filter Design

[10 hours]

Types of Digital Filters: FIR & IIR, FIR & IIR Filter Structures.

FIR Filter Design & Realization: Ideal filter requirements, Gibbs phenomenon, Characteristics and comparison of different window functions, Design of linear phase FIR filter: Fourier Series method, Rectangular, Hamming, Hanning & Blackman window function.

IIR Filter Design & Realization: Design of IIR filters from analog filters, IIR filter design by impulse invariance method, Bilinear transformation method. Characteristics of Butterworth filters, First & Second order Butterworth filter design.

Unit 5: Multirate DSP

[7 hours]

Concept of Multirate Signal Processing, Decimation, Interpolation, Sampling Rate Conversion by I/D, Polyphase Filters, Digital Filter Banks, Applications of Multirate DSP.

TEXTBOOKS:

1. John G. Proakis and Dimitris G. Manolakis, “Digital Signal Processing”, 4th Edition, Pearson Education. 2006
2. A. Nagoor Kani Digital Signal Processing, 2nd Edition, TMH Publication, 2012.

REFERENCES BOOKS:

1. S. K. Mitra, “Digital Signal Processing: A computer-based approach”, 3rd Edition, MC-Graw Hill publication.
2. A.V. Oppenheim and Schafer, Discrete Time Signal Processing, Prentice Hall, 1989.
3. L.R. Rabiner and B. Gold, Theory and Application of Digital Signal Processing, Prentice Hall, 1992.
4. Ramesh Babu, Digital Signal Processing, 4th Edition, Chennai Scitech Publications, 2011.

Final Year (Semester-VII)

Analog VLSI Design

BTEEV702	Analog VLSI Design	PCC-10	3L- 0T - 0P	3 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20 Marks Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Understand the fundamentals of CMOS analog circuit design and MOSFET device characteristics.
2. Illustrate fundamentals of current mirrors, bandgap reference circuits, and biasing techniques used in analog ICs.
3. Explain single-stage CMOS amplifiers and their performance characteristics.
4. Analyze the architecture, performance, stability, and frequency compensation of CMOS operational amplifiers.
5. Explore the design and application of advanced analog blocks, particularly Operational Transconductance Amplifiers (OTAs).

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the fundamentals of CMOS analog circuits and MOSFET characteristics.
CO2	Analyze current mirrors, bandgap reference circuits, and biasing techniques used in analog ICs.
CO3	Illustrate the operation and performance of single-stage CMOS amplifiers
CO4	Analyze the performance, stability, and frequency compensation of CMOS operational amplifiers.
CO5	Explain the design principles and applications of Operational Transconductance Amplifiers (OTAs).

Course Contents:

UNIT I: CMOS Analog building blocks

[08 Hours]

Necessity of CMOS analog design, MOS Models: Structure of MOSFET, Review of characteristics of MOS device, Second order effects, Short Channel Effects, MOS small signal model.

UNIT II: Current Mirrors and Bandgap References

[08 Hours]

Passive and Active Current Mirrors: Basic current mirrors, Cascode current mirrors and Active current mirrors, Band Gap References: General Considerations, Supply independent biasing, Temperature independent references, PTAT current generation and Constant Gm biasing.

UNIT III: Single Stage amplifiers

[08 Hours]

Basic concepts, Common source stage: resistive load, diode-connected load, current-source load, triode load and source degeneration, Source follower, Common gate stage, Cascode stage.

UNIT IV: MOS Operational Amplifiers

[08 Hours]

Op-amp: General Considerations, performance parameters, One-stage op-amps, Two-stage op-amps, Gain Boosting, Common-mode feedback, Input range limitations, Slew Rate, Power supply rejection.

Stability and Frequency Compensation: General Considerations, Multipole systems, Phase margin, Frequency compensation, compensation of two stage op-amps.

UNIT V: Operational Transconductance Amplifiers (OTA)**[08 Hours]**

Design of classical Op-Amps, Wide band Op-Amps, High Speed Op-Amps, Very High Gain Op-Amps, Operational Transconductance Amplifiers, Ultra Low Power OTAs for Medical Implants.

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001, 3rd re-print, 2016.
2. P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," 3rd Edition, Oxford University Press.

REFERENCES BOOKS:

1. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", John Wiley & Sons, Inc, Second Edition.
2. Phillip Allen and Douglas Holmberg "CMOS Analog Circuit Design" Second Edition, Oxford University Press, 2004.
3. A.S. Sedra and K. C. Smith, Adapted by A.N. Chandorkar, "Microelectronic Circuits-Theory & Applications" by 6th Edition, Oxford, 2013.
4. David Johns, Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.
5. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiley, 2009.

Final Year (Semester-VII)

VLSI Verification & Testing

BTEEV703	VLSI Verification & Testing	PCC-11	3L- 0T - 0P	3 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 0 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Understand the VLSI high-level design flow and high-level synthesis techniques.
2. Explain logic synthesis, optimization, and verification methods used in VLSI design.
3. Understand temporal logic and model checking techniques for hardware verification.
4. Analyze digital VLSI testing and Design for Testability (DFT) techniques.
5. Explore CMOS IC testing methods, including ATPG, scan testing, and Built-In Self-Test (BIST).

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the VLSI high-level design flow and high-level synthesis techniques.
CO2	Use logic synthesis, optimization, and verification methods for digital circuits.
CO3	Apply temporal logic and model checking techniques used in VLSI verification.
CO4	Analyze digital VLSI testing and Design for Testability (DFT) techniques.
CO5	Illustrate CMOS IC testing techniques, including ATPG, scan chain testing, and Built-In Self-Test (BIST).

Course Contents:

Unit 01: VLSI HIGH LEVEL DESIGN

[10 hours]

Introduction MOS and related VLSI technology, VLSI Design flows, Transformations for High Level Synthesis, Scheduling, Allocation and Binding, Introduction to HLS: Scheduling, Allocation and Binding Problem, Scheduling Algorithms, Binding and Allocation Algorithms

Unit 2: LOGIC SYNTHESIS AND VERIFICATION

[8 hours]

Logic Optimization and Synthesis, two level Boolean Logic Synthesis, Heuristic Minimization of Two-Level Circuits, Finite State Machine Synthesis, Multilevel Implementation Binary Decision Diagram: Introduction and construction, Ordered Binary Decision Diagram, Operations on Ordered Binary Decision Diagram.

Unit 3: TEMPORAL LOGIC AND MODEL CHECKING

[8 hours]

Introduction and Basic Operations on Temporal Logic, Syntax and Semantics of CLT, Equivalence between CTL Formulas, Verification Techniques, Model Checking Algorithm, Symbolic Model Check.

Unit 4: Digital VLSI testing and DFT

[7 hours]

Introduction to Digital VLSI Testing, Functional and Structural Testing, Fault Equivalence, Fault Simulation and Testability Measures. (Verilog)

Unit 5: CMOS IC TESTING

[7 hours]

Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras, D-Algorithm, ATPG for Synchronous Sequential Circuits, Scan Chain based Sequential Circuit Testing, Built in Self-Test, Memory Testing.

Textbooks:

1. Basic VLSI design by Douglas A, Pucknell, Kamran Eshraghian, Prantice Hall, 1996 3rd edition.
2. VLSI DESIGN - K. Lal Kishore, V.S.V Prabhakar, I.K International, 2009.
3. CMOS VLSI Design- Neil H.E Weste, David Harris, Ayan Banerjee, Pearson Education, 1999.
4. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.

Reference Books:

1. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
2. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
3. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004.
4. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000

Final Year (Semester-VII)

Professional Elective Course-IV

A) Low Power VLSI Design

BTEEV704A	Low Power VLSI Design	PEC-4	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. To understand the fundamentals of low-power VLSI design and power dissipation mechanisms in CMOS circuits.
2. To study low-power design methodologies through voltage scaling and switching activity optimization.
3. To illustrate low-voltage, low-power adder architectures used in VLSI systems.
4. To explore low-power multiplier design techniques and their architectures.
5. To understand semiconductor memory design and low-power operation of ROM, SRAM, and DRAM circuits.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the sources of power dissipation in digital IC systems & the impact of power on system performance and reliability.
CO2	Illustrate the different low-power design approaches and optimization of switched capacitance.
CO3	Discuss the different low-power high speed adders.
CO4	Apply the concepts of low voltage and low power to different multipliers.
CO5	Apply the concepts of low voltage and low power to different memories.

Course Contents:

UNIT I: Fundamentals of Low Power VLSI Design **[08 Hours]**

Need for Low Power Circuit Design, Sources of Power Dissipation- Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation-Reverse diode leakage current, Sub threshold leakage current, Glitching Power Dissipation.

UNIT II: Low-Power Design through Voltage Scaling **[08 Hours]**

VTCMOS circuits, MTCMOS circuits, Architectural Level Approach - Pipelining and Parallel Processing Approaches.

Estimation and Optimization of Switching Activity

The Concept of Switching Activity, Reduction of Switching Activity, Reduction of Switched Capacitance-System Level Measures, Circuit Level Measures, and Mask level Measures.

UNIT III: Low-Voltage Low-Power Adders **[08 Hours]**

Introduction, Standard Adder Cells, CMOS Adder's Architectures - Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Carry Skip Adders.

UNIT IV: Low-Voltage Low-Power Multipliers **[08 Hours]**

Overview of Multiplication, Booth Multiplier-Booth's algorithm, modified Booth algorithm, Introduction to Tree Multiplier (Wallace and Dada multipliers) and 4:2 Compressors.

UNIT V: Semiconductor Memories**[08 Hours]**

Introduction, Read Only Memory circuits, Static Read-Write Memory circuits-SRAM operation principles, Full CMOS SRAM Cell, SRAM write circuitry, SRAM read circuitry, Dynamic Read-Write Memory circuits, DRAM Cells- Three and One transistor DRAM Cells.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, Low-Voltage, Low-Power VLSI Subsystems, TMH Professional Engineering., 7th Edition, 2004

REFERENCES BOOKS:

1. Anantha Chandrakasan, Low Power CMOS Design, IEEE Press/Wiley International, 1998.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, Kluwer Academic Press, 2002.
3. Kaushik Roy, Sharat C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley & Sons, 2000.
4. Ajit Pal, Low-Power VLSI Circuits and Systems, Springer, August 2016.

Final Year (Semester-VII)

B) Semiconductor Packaging and Testing

BTEEV704B	Semiconductor Packaging and Testing	PEC-4	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

1. Understand the fundamentals of semiconductor packaging technologies, package types, and packaging materials used in integrated circuits.
2. Explain semiconductor package manufacturing processes, including assembly, interconnection, and encapsulation techniques.
3. Develop knowledge of semiconductor testing methods, failure analysis, and reliability assessment for ensuring product quality.
4. Apply quality control principles and gain awareness of advanced semiconductor packaging technologies and emerging industry trends.
5. Explore advanced packaging technologies and current industry trends.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain semiconductor packaging technologies and package materials.
CO2	Describe semiconductor package manufacturing and assembly processes.
CO3	Illustrate semiconductor testing methods and failure analysis techniques.
CO4	Apply quality control and statistical process control in semiconductor manufacturing.
CO5	Discuss advanced packaging technologies and current industry trends.

Course Contents:

Unit 1: Introduction to Semiconductor Packaging **[09 Hours]**

Introduction to semiconductor packaging, assembly flow, packaging history, package families, package functions, need for packaging, and overview of packaging materials and technologies.

Unit 2: Semiconductor Package Manufacturing **[08 Hours]**

Wafer thinning, dicing, die attach, wire bonding, flip-chip packaging, encapsulation, solder ball attachment, reflow process, singulation, laser marking, cleanroom practices, and packaging equipment.

Unit 3: Semiconductor Testing and Failure Analysis **[08 Hours]**

Testing methodologies, functional and parametric testing, automated test equipment, wafer probing, burn-in testing, reliability testing, failure modes, failure analysis, ESD and EMI protection, and test data analysis.

UNIT 4: Quality Control and Process Management **[08 Hours]**

Quality Control (QC), Quality Management System (QMS), incoming and in-process inspection, Statistical Process Control (SPC), process capability, Fault Detection and Classification (FDC), Run-to-Run (R2R) control, and defect analysis.

Unit 5: Advanced Packaging Technologies **[07 Hours]**

Wafer-Level Packaging (WLP), System-in-Package (SiP), 2.5D/3D packaging, Through Silicon Via (TSV), heterogeneous integration, advanced interconnects, thermal management,

With effective from academic year 2024-25

AI applications in testing, and future packaging trends.

TEXTBOOKS

1. Fundamentals of Microsystems Packaging Tummala, Rao R., McGraw Hill, 2001.
2. The electronic packaging handbook Blackwell (Ed), CRC Press, 2000.
3. Microelectronics packaging handbook Tummala, Rao R, McGraw Hill, 2008.

REFERENCE BOOKS

1. Printed Circuit Boards Design and Technology Bosshart TataMcGraw Hill, 1988.
2. Electronic Product Design R.G. Kaduskar and V.B.Baru Wiley India, 2011
3. Printed Circuit Board R.S.Khandpur Tata McGraw Hill, 2005
4. Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits Michael L. Bushnell & Vishwani D. Agrawal Kluwer Academic Publishers.2000
5. Digital System Testing and Testable Design M. Abramovici, M. A. Breuer, and A.D. Friedman Computer Science Press,1990

Final Year (Semester-VII)

C) System on Chip

BTEEV704C	System On Chip	PEC-4	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. To introduce the fundamental concepts, terminology, and principles of the subject.
2. To develop an understanding of the core techniques, methodologies, and processes used in the subject.
3. To familiarize students with the operation and applications of the subject in engineering practice.
4. To develop the ability to analyze basic engineering problems using appropriate concepts and methods.
5. To enable students to apply the acquired knowledge and techniques to solve simple engineering problems.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the architecture, components, design methodology, benefits, challenges, and applications of System-on-Chip (SoC) technology.
CO2	Describe the architecture and characteristics of SoC processors, including processor selection, instruction handling, pipelining, vector, VLIW, and superscalar processors.
CO3	Interpret the organization of SoC buses, AMBA protocols, CoreConnect architecture, ST bus protocols, and memory hierarchy used in SoC systems.
CO4	Apply the concepts of processor architecture, instruction set design, RISC principles, and low-power techniques in processor design.
CO5	Apply ARM processor architecture, programming model, pipelining, debugging interfaces, co-processors, floating-point architecture, and hardware prototyping tools in SoC-based system design.

Course Contents:

Unit I - Introduction to SOC

[08 Hours]

System Architecture, System Complexity, Components of the system Hardware & Software, An approach for SOC Design, SOC definition, benefits and challenges, Application of SOC, SOC components: Processor, Accelerators, Memory and Peripherals, On-chip interconnects, and various signal processing units.

Unit II - SOC Processors

[08 Hours]

Introduction to SOC processors, Processor selection for SOC, Basic concepts in processor architecture and processor micro architecture, Basic elements in Instruction handling, Buffers: minimizing pipeline delays Branches, More Robust Processors: Vector processors and vector instructions extensions, VLIW Processors, Superscalar Processors.

Unit III - SOC Buses and Memory

[08 Hours]

AMBA: Generation of AMBA (ASB AHB APB) Architecture of AMBA Specification, Core Connect bus: PLB OPB DCR; ST bus protocols: Type I, II, III; SOC memory, Cache memory: performance partitioning multi-level cache; Memory chip technology: On die or Off die.

UNIT-IV - Introduction to Processor Design

[08 Hours]

Processor architecture and organization, Abstraction in hardware design, MU0 – a simple processor, Instruction set design, Processor design trade-offs, RISC, Design for low power consumption.

With effective from academic year 2024-25

UNIT-V - ARM Processor as System-On-Chip

[08 Hours]

Acorn RISC Machine, Architectural inheritance, ARM programmer's model, ARM development tools, 3 and 5 stage pipeline ARM organization, ARM instruction execution and implementation, ARM Co-processor interface, ARM Floating Point Architecture, Hardware System Prototyping Tools, JTAG Boundary scan test architecture, ARM debug architecture.

Textbooks:

1. Michael J. Flynn Wayne Luk "Computer System Design: System on Chip" John Wiley and sons.
2. Steve Furber "*ARM system on chip Architecture*" 2nd ed. Pearson 2000.

Reference Books:

1. M.Wolf "Principles of Embedded Computing System Design" 4th Edition Morgan Kaufmann Publications.
2. Prakash Rashinkar Peter Paterson and Leena Singh L. "System on Chip Verification – Methodologies and Techniques" Kluwer Academic Publisher 2001.
3. Ricardo Reis "Design of System on a Chip: Devices and Components" 1st ed. Springer 2004.

Final Year (Semester-VII)

D) Quantum Computing

BTEEV704D	Quantum Computing	PEC-4	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

1. To discuss Superposition and Single Qubit.
2. To explore 1-qubit and 2-qubit gate operations.
3. To explore the basics of Linear Algebra for analyzing Two-qubit gates.
4. To discuss the concepts of entanglement.
5. To discuss Simple Quantum Algorithms.

Course Outcomes: After completion of the course, students will be able to:

CO1	Understand Superposition and Single Qubit.
CO2	Understand different Quantum Gates.
CO3	Explore operation of 1-qubit and 2-qubit gate using Basics of Linear Algebra.
CO4	Understand Entanglement and testing for entangled states.
CO5	Illustrate Simple Quantum Algorithms.

Course Contents:

Unit 1: Introduction to Quantum computing

[08 Hours]

Elementary quantum mechanics: linear algebra for quantum mechanics, Quantum states in Hilbert space, The Bloch sphere, Density operators, generalized measurements, no-cloning theorem.

Unit 2: Quantum Gates and Circuits

[08 Hours]

Model of computation (movement on Bloch Sphere), X, Y, Z, H gates, CNOT, Toffoli, Fredkin, SWAP gate, Simple circuits, Quantum Adder, Reversible circuits.

Unit 3: Quantum correlations

[08 Hours]

Bell inequalities and entanglement, Schmidt decomposition, superdense coding, teleportation.

UNIT 4: Entanglement

[08 Hours]

Entangled States, Testing for Entangled States, Bell Pair and Bell States, EPR Paradox & Bell Theorem, Conditional Instructions, Quantum Teleportation, Superdense Coding.

Unit 5: Simple Quantum Algorithms

[08 Hours]

Deutsch, Deutsch-Jozsa, Bernstein Vazirani, Grover, Shor's Algorithm.

TEXTBOOKS

1. Philip Kaye, Raymond Laflamme et. al., An introduction to Quantum Computing, Oxford University press, 2007.
2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, Cambridge, 2020.
3. David McMahon-Quantum Computing Explained-Wiley-Interscience, IEEE Computer Society (2008).

REFERENCE BOOKS

1. Quantum Computation and Quantum Information, M. A. Nielsen & I. Chuang, Cambridge University Press (2013).
2. Quantum Computing, A Gentle Introduction, Eleanor G. Rieffel and Wolfgang H. Polak MIT press (2014).

Final Year (Semester-VII)

Open Elective Course (OEC) – III

A) Deep Learning & Data Sciences

BTEEV705A	Deep Learning & Data Sciences	OEC-3	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives:

1. Understand the fundamentals of neural networks and deep learning techniques.
2. Explain the architecture and working of Convolutional Neural Networks (CNNs).
3. Understand transfer learning and effective training techniques for deep neural networks.
4. Apply data science concepts for data preprocessing, analysis, and visualization.
5. Explore data manipulation techniques and applications of data science, including web scraping and natural language processing.

Course Outcomes: After completion of the course, students will be able to:

CO1	Apply neural network models and optimization techniques to solve basic machine learning problems.
CO2	Illustrate Convolutional Neural Networks (CNNs) for image and video classification tasks.
CO3	Apply transfer learning and effective training techniques to improve deep learning model performance.
CO4	Use data science tools and Python libraries for data preprocessing, analysis, and visualization.
CO5	Apply data manipulation, exploratory data analysis, and text processing techniques to solve real-world data science problems.

Course Contents:

Unit 1: Introduction to Neural Networks

[08 Hours]

Basic Mathematics: Scalar and Vector Matrices, Eigen Values, Matrix Multiplication and Eigen Vectors.

Neural Networks: Introduction and Working of Simple Artificial Neural Network, Multilayer Perceptron, Forward Propagation and Back Propagation Learning, Building Blocks of Deep Neural Networks, Optimization Techniques, Gradient Descent and its variants, Derivatives, Batch Optimization, Momentum Optimizer, RMSProp, Adam, Vectorization, Linear Regression and Logistic Regression with Deep Neural Network.

Unit 2: Convolutional Neural Networks

[08 Hours]

Introduction Convolutional Neural Network, Fully Connected Network vs Convolutional Neural Network, Building Blocks Of CNN: Filters, Convolution, Pooling, Activations Etc. Training Procedure of CNN, Feeding Images and Videos to CNN, Different CNN Architectures, Residual Networks, Skip Connections.

Unit 3: Transfer Learning and Effective training in Deep Net:

[08 Hours]

Transfer Learning: Introduction To Transfer Learning, Need for Transfer Learning, Feature Extraction Using Transfer Learning, Fine Tuning. Effective Training: Bias Variance Tradeoff, Dealing with Overfitting and Underfitting, Data Augmentation, Early Stopping, Dropout, Batch Normalization, Instance Normalization, Group Normalization, Regularization, Hyperparameter Tuning.

Unit 4: Fundamentals of Data Science**[08 Hours]**

Introduction to Data Science, Data Science Life Cycle, Types of Data, Data Collection and Data Acquisition, Data Cleaning and Data Preprocessing, Handling Missing Values and Outliers, Data Transformation and Feature Engineering, Exploratory Data Analysis (EDA), Descriptive Statistics, Data Visualization using Matplotlib and Seaborn, Introduction to Predictive Analytics, Python Libraries for Data Science (NumPy, Pandas, Scikit-learn).

Unit 5: Manipulation of Data and Applications**[08 Hours]**

Data Wrangling, Data manipulation, Plotting- Visualization with ggplot2, Statistical inference, What-if analysis. Exploratory Data Analysis and the Data Science Process, Basic tools (plots, graphs and summary statistics) of EDA. Web scraping, Text data and Natural Language Processing.

TEXTBOOKS:

1. Deep Learning: A Practitioner's Approach, Josh Patterson, Adam Gibson, O'Reilly Media, 2017.
2. James Allen “Natural Language Understanding”, Pearson Publication 8th Edition. 2012.
3. François Chollet “Deep Learning with Python,” First Edition, Manning Publication, 2018

REFERENCE BOOKS:

1. Cathy O'Neil and Rachel Schutt. Doing Data Science, Straight Talk from The Frontline. O'Reilly. 2014.
2. Foster Provost and Tom Fawcett. Data Science for Business: What You Need to Know about Data Mining and Data-analytic Thinking. ISBN 1449361323. 2013.
3. Martin Bruschler, Thilo Stadelmann, Kurt Stockinger Applied Data Science Lessons Learned for the Data-Driven Business, Springer 2019.

Final Year (Semester-VII)

B) Linux OS

BTEEV705B	Linux OS	OEC-3	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week	Continuous Assessment: 20 Marks
Tutorial: 1 hr./week	Mid Semester Exam: 20 Marks
	End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. To understand the basic concepts, structure, and functions of operating systems.
2. To develop knowledge of process, memory, and file management in a simplified manner.
3. To introduce Linux operating system and its command-line environment.
4. To enable students to perform basic file, process, and system operations using Linux.
5. To apply Linux commands and utilities for real-world engineering tasks and problem-solving.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the basic concepts, types, and structure of operating systems and perform basic Linux commands.
CO2	Illustrate process management concepts and use Linux commands to monitor and manage system processes.
CO3	Describe basic memory management and deadlock concepts and observe system performance using Linux tools.
CO4	Explain file system, device, and storage concepts and perform file handling and permission operations in Linux.
CO5	Apply Linux commands for file management, data handling, process monitoring, and basic automation in engineering tasks.

Course Contents:

Unit 01: Fundamentals of Operating Systems and Linux [9 hours]

Operating System Basics: Concept and functions of Operating System, Components of OS (Kernel, Shell – basic idea), Types of OS: Batch, Time-sharing, Real-time, Distributed (overview only), User view vs System view (simple explanation), OS services (file, process, memory – basic idea).

Introduction to System Calls (concept only, no coding).

Computer System Overview: Single processor vs multiprocessor (basic idea)

Process Introduction: What is a process? Basic process states (new, ready, running, waiting, terminated), Introductory, running to threads (only concept)

Linux: Introduction to Linux, Basic Linux commands (ls, cd, pwd, mkdir, rm)

Unit 2: Linux Environment and Command Line Operations [8 hours]

Process Synchronization (Concept Only): Need for synchronization, Critical section problem (basic idea), Simple explanation of synchronization tools (no algorithms)

CPU Scheduling (Very Basic): What is CPU scheduling?, Goals: fairness, efficiency, Basic idea of common methods: FCFS, Round Robin (No numerical problems, no multilevel queues)

Linux: Process-related commands: ps, top, kill, Basic idea of system calls in Linux

Unit 3: File System Management and Permissions in Linux [7 hours]

Deadlock: What is deadlock? Causes of deadlock (4 conditions), Basic prevention ideas.

Memory Management: What is memory management? Primary vs secondary memory.

Basics of Paging, Segmentation, Virtual memory.

Linux: Memory-related basic commands: free, top.

Unit 4: Process and Memory Management Concepts**[8 hours]**

File System: Concept of File and its types, Directory structure, File operations (create, delete, read, write), File allocation.

Devices & Storage: Types of devices (input/output), Disk storage, Disk management.

Linux: File management commands: cp, mv, rm, cat, Directory management, File permissions (chmod – basic).

Unit 5: Use of Linux in Engineering Tasks**[8 hours]**

File and Project Management in Linux: Organizing engineering project directories and files, creating, copying, moving and deleting files (mkdir, cp, mv, rm), viewing and managing output files (cat, less). Data Handling and Searching Techniques: Searching files using find, extracting useful data using grep, use of pipes (|) for combining commands.

Process and System Resource Management: Monitoring running processes (ps, top), managing processes (kill), basic idea of CPU and memory usage. Command Automation and Output Management: Basic command chaining, input/output redirection (>, >>), repetitive task handling using simple command sequences.

Textbooks:

1. Silberschatz, Galvin, Greg, “Operating System Concepts”, Wiley and Sons, 9th Edition, 2015.
2. Sumitabha Das, “UNIX Concepts and Applications”, McGraw Hill Education, 4th Edition.
3. Richard Petersen, “Linux: The Complete Reference”, McGraw Hill Education, Latest Edition.
4. Herbert Schildt, “Java: The complete reference”, Tata McGraw Hill, 7th Edition.

Reference Books:

1. Achyut S. Godbole, “Operating Systems”, McGraw Hill Education, 2nd Edition.
2. Andrew S. Tanenbaum, “Modern Operating Systems”, Pearson Education, 3rd Edition.
3. William Stallings, “Operating Systems: Internals and Design Principles”, Pearson, 9th Edition.
4. Kenneth H. Rosen et al., “UNIX: The Complete Reference”, McGraw Hill, 6th Edition.

Final Year (Semester-VII)

C)Cyber Security

BTEEV705C	Cyber Security	OEC-3	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. Understand the fundamentals of cyber security, cyber threats, and security mechanisms.
2. Explain cryptographic concepts and encryption techniques for secure communication.
3. Understand cryptographic algorithms, hash functions, and digital signature techniques.
4. Apply security mechanisms for securing e-mail and network communications.
5. Explore web security principles, intrusion detection, firewalls, and protection against cyberattacks.

Course Outcomes: After completion of the course, students will be able to:

CO1	Understand fundamental cyber security principles to identify and mitigate common security threats and attacks.
CO2	Use cryptographic techniques to secure data through encryption and decryption.
CO3	Apply cryptographic algorithms, hash functions, and digital signatures to ensure secure communication.
CO4	Illustrate e-mail and network security mechanisms using standard security protocols.
CO5	Apply web security techniques, intrusion detection methods, and firewall mechanisms to protect information systems.

Course Contents:

Unit I: Introduction to Cyber Security

[08 Hours]

Introduction, The need for security, Security approaches, Principles of security, Types of Security attacks, Security Mechanisms, A model for Network Security. Cyber threats, Cyber-crimes and laws, Information Technology Act 2000.

Unit II: Cryptography-Concepts and Techniques

[08 Hours]

Introduction, plain text and cipher text, substitution techniques, transposition techniques, encryption and decryption, symmetric and asymmetric key cryptography, stenography, key range and key size, possible types of attacks.

Unit III: Cryptographic Algorithms and Hash Function

[08 Hours]

Block Cipher principles & Algorithms (DES, AES, Blowfish), Differential and Linear Crypt analysis, Asymmetric key Ciphers, Principles of public key crypto systems, Algorithms (RSA, Diffie Hellman). Hash Functions, Secure Hash algorithm, Digital signatures.

Unit IV: E-Mail Security

[08 Hours]

Pretty Good Privacy, S/MIME, IP security overview, IP Security architecture, Authentication Header, Encapsulating, Security payload, Combining security associations, Key management.

Unit V: Web Security

[08 Hours]

Web security considerations, Secure Socket Layer and Transport Layer Security, Secure electronic transaction, Intruders, Intrusion detection, password management, virus and related threats, Countermeasures, Firewall design principles, types of firewalls, Secure Inter-branch Payment Transactions, Cross site Scripting.

Text Books:

1. William Stallings , “Cryptography and Network Security” ,Pearson Education, 4th Edition
2. Atul Kahate, “Cryptography and Network Security”, McGraw Hill, 3rd Edition.
3. C K Shymala, N Harini, Dr. T R Padmanabhan, “Cryptography and Network Security”, Wiley India, 1st Edition.

Reference Books:

1. Forouzan Mukhopadhyay, “Cryptography and Network Security”, Mc Graw Hill, 2nd Edition.
2. Mark Stamp, “Information Security, Principles and Practice”, Wiley India, 2nd Edition.
3. W.M. Arthur Conklin, Greg White, “Principles of Computer Security”, TMH, 4th Edition.
4. Neal Krawetz, “Introduction to Network Security”, CENGAGE Learning Distributor, 1st Edition.
5. Bernard Menezes, “Network Security and Cryptography”, CENGAGE Learning Distributor, 1st Edition.

Final Year (Semester-VII)

D)Advanced Communication Technology

BTEEV705D	Advanced Communication Technology	OEC-3	3L- 1T - 0P	4 Credits
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Teaching Scheme	Examination Scheme
Lecture: 3 hrs./week Tutorial: 1 hr./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Pre-requisite: Basics of Advanced Communication Technology.

Course Objectives: The aim of this course is to:

1. Explain the principles of satellite communication, orbital mechanics, and satellite system components.
2. Describe satellite-based communication services, navigation systems, and GPS technology.
3. Illustrate the operating principles and transmission characteristics of optical fiber communication.
4. Interpret the working of optical sources, detectors, and modern optical communication devices.
5. Summarize the architecture, technologies, and applications of 5G wireless communication.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the concepts of satellite communication, orbital parameters, satellite transponders, and propagation characteristics.
CO2	Describe the architecture and operation of VSAT systems, GPS, and satellite navigation services.
CO3	Illustrate the principles of optical fiber propagation, transmission characteristics, and wavelength division multiplexing.
CO4	Interpret the operating principles of optical sources, semiconductor lasers, LEDs, and optical detectors.
CO5	Summarize the architecture, key technologies, and applications of 5G communication, IoT integration, and Massive MIMO.

Course Contents:

UNIT I: Satellite Communication

[08 Hours]

Satellite frequency bands, Satellite types-LEO, MEO, GEO, HEO, Uplink, Downlink, Cross link, Kepler's laws, Satellite orbits, Geo-stationary Satellite. Orbital Aspects of Satellite Communication: Orbital period and velocity, Effect of orbital inclination, Azimuth and Elevation, Converge angle and Slant range, Satellite Transponder, Electromagnetic field Propagation, Atmospheric Losses, Receiver noise, Carrier to noise ratio, Frequency reuse and depolarization.

UNIT II: Satellite Services

[08 Hours]

Very Small Aperture Satellite (VSAT): Overview of VSAT system, Network architecture, VSAT antennas, Transmitter and Receiver. Satellite Navigation and Global Positioning System (GPS): Radio and Satellite navigation, Position, Location in GPS, GPS receivers and codes, GPS navigation message and signal levels, Timing accuracy, GPS receiver operation.

UNIT III: Optical Fiber Waveguide and Transmission Characteristics

[08 Hours]

Ray Theory of Optical Fiber, Total internal reflection, Snell's law, Acceptance Angles, Numerical Aperture (NA), Modes in Optical Fiber, Single mode and Multimode Optical Fiber, Power flow. Transmission Characteristics of Optical Fiber: Attenuation, Absorption losses, scattering losses, Bending losses, Dispersion, Intermodal and Intramodal Dispersion; Concept of Wavelength Division Multiplexing.

UNIT IV: Optical Sources and Detectors**[08 Hours]**

Optical Sources: Optical Emission from Semiconductor, LED, Power, Efficiency, Double heterojunction LED, Basic concept of LASER, Semiconductor injection LASER.

Optical Detectors: Optical detection principle, Absorption, quantum efficiency, Responsivity, PIN Photodiode, Avalanche Photodiode and Phototransistor.

UNIT V: Introduction to 5G Technology**[08 Hours]**

Historical trend and evolution of LTE technology to beyond 4G – Key building blocks of 5G, Specification requirements for driving 5G technology, 5G Use Cases and System Concepts – The 5G Architecture – IoT in relation to 5G; Massive MIMO: Fundamentals, Advantages.

TEXTBOOKS:

- 1) Gagliardi Robert M.: “Satellite Communication”, CBS Publication and Distributors, New Delhi
- 2) Senior J.M.: “Optical Fiber communication and Application”, Prentice Hall of India Pvt. Ltd, New Delhi.
- 3) Wei Xiang, Kan Zheng, Xuemin (Sherman) Shen, - 5G Mobile Communications, Springer, 2017.

REFERENCE BOOKS

- 1) Goward: “Optical Communication System”, Prentice Hall.
- 2) R. P. Khare: “Fiber Optics and Opto Electronics”, Oxford University Press, First Edition.
- 3) G. Keiser: “Optical Fiber Communication”, McGraw Hill International Book Co. New York.
- 4) Pratt Timothy and Bostian W. Charles: “Satellite Communication”, Wiley International Publication, New York.
- 5) Afif Osseiran, Jose F. Monserrat and Patrick Marsch, - 5G Mobile and Wireless Communications Technology, Cambridge University Press, 2016.

Final Year (Semester-VII)

Humanities and Social Sciences including Management

Elective Course (HSSMEC)- II

A) Foreign Language Studies

BTEEV706A	Foreign Language Studies	HSSMEC-6	1L- 1T - 0P	Audit
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Teaching Scheme	Examination Scheme
Lecture: 1 hr./week Tutorial: 1 hr./week	Audit

Course Objectives: The aim of this course is to:

1. Introduce students to basic German language communication.
2. Develop Listening, Speaking, Reading, and Writing (LSRW) skills in German.
3. Enhance global employability, intercultural competence, and professional communication skills.

Course Outcomes: After completion of the course, students will be able to:

CO1	Understand basic German vocabulary, pronunciation, and grammar structures.
CO2	Communicate simple ideas and everyday conversations in German.
CO3	Interpret basic German texts and messages.
CO4	Demonstrate awareness of German culture and social etiquette.
CO5	Apply basic German language skills in academic, professional, and international environments.

Course Contents:

Unit I: Basics of Language **[10 Hours]**

German alphabet and pronunciation, Greetings and farewells, Self-introduction, Introducing others, Numbers (0–100), Days, months, dates, and time.

Unit II: Basic Grammar and Vocabulary **[8 Hours]**

Introduction, Sentence formation, Basic tenses, Articles, pronouns, verbs.

Unit III: Communication Skills **[6 Hours]**

Introduction, Everyday conversations, Asking directions, Shopping / travel dialogues

Unit IV: Reading & Writing **[8 Hours]**

Reading simple passages and dialogues, Letter / email writing, Vocabulary building.

Unit V: Culture & Application **[8 Hours]**

Introduction to German-speaking countries, German customs, traditions and festivals, Intercultural communication, German in engineering and technology sectors, Basic professional communication

Textbooks:

1. “*German Made Simple*”, Author: Arnold Leitner, Publisher: Broadway Books
2. “*Menschen A1*”, Authors: Susanne Kalender, Paul Rusch, Helen Schmitz, et al, Publisher: Hueber Verlag
3. “*Netzwerk Neu A1*”, Authors: Stefanie Dengler, Paul Rusch, Tanja Mayr-Sieber, Publisher: Klett Verlag

Reference Books:

1. *“Schritte International Neu A1”*, Publisher: Hueber Verlag
2. *“Studio d A1”*, Authors: Hermann Funk, Christina Kuhn, Publisher: Cornelsen Verlag
3. *“Essential German Grammar”*, Author: Guy Stern, Publisher: Dover Publications

Final Year (Semester-VII)

B) Universal Human Value & Ethics

BTEEV706B	Universal Human Value & Ethics	HSSMEC-6	1L- 1T - 0P	Audit
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Teaching Scheme	Examination Scheme
Lecture: 1 hr./week Tutorial: 1 hr./week	Audit

Course Objectives: The aim of this course is to:

1. Understand the basic human aspirations and the concept of all-encompassing resolution for achieving harmony in life.
2. Explain the concepts of right understanding, self-exploration, and the relationship between the self, body, and human existence.
3. Understand the relation and co-existence of human beings, nature, and the entire existence.
4. Recognize the importance of ethical human conduct, self-awareness, and responsible participation in society.
5. Apply the principles of holistic living and universal human values for achieving harmony at individual, family, societal, and environmental levels.

Course Outcomes: After completion of the course, students will be able to:

CO1	Explain the basic human aspirations and the concept of all-encompassing resolution for harmonious living.
CO2	Interpret the concepts of right understanding, self-exploration, and the relationship between the self and the body
CO3	Explain the principles of self-awareness and understanding of human existence to promote harmony within oneself and with others
CO4	Explain the relation of human beings, nature, and existence, and recognize the need for sustainable and harmonious coexistence
CO5	Illustrate the principles of ethical human conduct and holistic living to contribute towards a humane society and sustainable development

Course Contents:

Unit 1: Introduction-Basic Human Aspiration, its fulfilment through All-encompassing Resolution [09 Hours]

The basic human aspirations and their fulfilment through Right understanding and Resolution, Right understanding and Resolution are the activities of the self, self is central to Human Existence; All-encompassing Resolution for a Human Being, its details and solution of problems in the light of Resolution

Unit 2: Right Understanding (Knowing)- Knower, Known & the Process [08 Hours]

The domain of right understanding starts from understanding the human being (the knower, the experiencer and the doer); and extends up to understanding nature/existence – its interconnectedness and co-existence; and finally understanding the role of human beings in existence (human conduct).

Unit 3: Understanding Human Being [08 Hours]

Understanding the human being comprehensively is the first step and the core theme of this course; human being as co-existence of the self and the body; the activities and potentialities of the self; Reasons for harmony/contradiction in the self.

Unit 4: Understanding Existence (including Nature) [08 Hours]

A comprehensive understanding (knowledge) about the existence, which certainly includes the Nature. The need and the process of inner evolution (through self-exploration, self-

awareness and self-evaluation)- particularly awakening to activities of the self: Realization, Understanding and Contemplation in the self (Realization of Co-Existence, Understanding of Harmony in Nature and Contemplation of Participation of Human in this harmony/ order leading to comprehensive knowledge about the existence).

Unit 5: Understanding Human Conduct and Holistic Way of Living [07 Hours]

Understanding different aspects of All-encompassing Resolution (understanding, wisdom, science etc.), Holistic way of living for Human Being with All-encompassing Resolution covering all four dimensions of human endeavor viz., realization, thought, behavior and work (participation in the larger order) leading to harmony at all levels from self to Nature and entire Existence, ultimately, leading to a Humane Society and Human Tradition.

Textbooks:

1. A Foundation Course in Human Values and Professional Ethics, R R Gaur, R Asthana, G P Bagaria, 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-87034-47-1
2. Avartansheel Arthshastra, A. Nagraj, Divya Path Sansthan, Amarkantak, India
3. Economy of Permanence – (a quest for social order based on non-violence), J. C. Kumarappa (2010), Sarva-Seva-Sangh-Prakashan, Varansi, India
4. Energy and Equity, Ivan Illich (1974), The Trinity Press, Worcester & Harper Collins, USA

Reference Books:

1. Ishadi Nau Upnishad, Shankaracharya, Geeta press, Gorakhpur,
2. Manav Vyavahar Darshan, A. Nagraj, Divya Path Sansthan, Amarkantak, India
3. Manaviya Samvidhan, A. Nagraj, Divya Path Sansthan, Amarkantak, India
4. Mahasatipatthan Sutta, S N Goenka, Vipassana Research Institute, First Edition, 1996
5. Small Is Beautiful: A Study of Economics as if People Mattered, E. F. Schumacher, 1973, Blond & Briggs, UK
6. Science & Humanism – towards a unified worldview, P. L. Dhar & R. R. Gaur (1990), Commonwealth Publishers, New Delhi
7. Sanchian Sri Guru Granth Sahib Ji, Shiromani Gurdwara Parbhandhak Committee, 2001
8. Saman Suttam, Jinendra Varni ,1974.
9. Vyavaharvadi Samajshastra, A. Nagraj, Divya Path Sansthan, Amarkantak, India
10. Vyavahatmak Janvad, A. Nagraj, Divya Path Sansthan, Amarkantak, India.

Final Year (Semester-VII)

C) Intellectual Property Rights

BTEEV706C	Intellectual Property Rights	HSSMEC-6	1L- 1T - 0P	Audit
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Teaching Scheme	Examination Scheme
Lecture: 1 hr./week Tutorial: 1 hr./week	Audit

Course Objectives: The aim of this course is to:

1. Understand the fundamentals of Intellectual Property Rights (IPR) and their significance.
2. Explain the concepts of patents and copyrights and their legal provisions.
3. Understand the registration and protection of trademarks.
4. Explain the importance of industrial designs and layout design protection.
5. Understand the provisions of the Information Technology Act, 2000 and its role in cyber law.

Course Outcomes: After completion of the course, students will be able to:

CO1	Understand the fundamental concepts of Intellectual Property Rights to identify different forms of intellectual property.
CO2	Use patent and copyright provisions to protect inventions and creative works.
CO3	Apply trademark laws and registration procedures to safeguard brands and domain names.
CO4	Apply design protection principles and layout design regulations for industrial and semiconductor products.
CO5	Discuss the provisions of the Information Technology Act, 2000 to address legal issues related to e-commerce, digital signatures, and cybercrimes.

Course Contents:

UNIT I: Introduction to IPR:

[08 Hours]

Meaning of property, Origin, Nature, Meaning of Intellectual Property Rights Introduction to TRIPS and WTO. Kinds of Intellectual property rights—Copy Right, Patent, Trademark, Trade Secret and trade dress, Design, Layout Design, Geographical Indication, Plant Varieties and Traditional Knowledge.

UNIT II: Patent Rights and Copy Rights

[08 Hours]

Patents: Origin, Meaning of Patent, Types, Inventions which are not patentable, Registration Procedure, Rights and Duties of Patentee, Assignment and license, Restoration of lapsed Patents, Surrender and Revocation of Patents, Infringement, Remedies & Penalties.

Copyrights: Origin, Definition & Types of Copy Right, Registration procedure, Assignment & license, Terms of Copyright, Piracy, Infringement, Remedies, Copyrights with special reference to software.

UNIT III: Trademarks

[08 Hours]

Origin, Meaning & Nature of Trademarks, Types, Registration of Trademarks, Infringement & Remedies, Offences relating to Trademarks, Passing Off, Penalties. Domain Names on cyber space.

UNIT IV: Design

[08 Hours]

Meaning, Definition, Registration of Design, Cancellation of Registration, International Convention on Design, Functions of Design. Semiconductor Integrated circuits and layout design Act-2000.

UNIT V: Information Technology Act-2000

[08 Hours]

IT Act – Introduction, E-Commerce and legal provisions, E- Governance and legal provisions, Digital signature and Electronic Signature, Cybercrimes.

TEXT BOOKS

1. Intellectual Property Rights: Unleashing the Knowledge Economy – Prabuddha Ganguli
2. Law Relating to Intellectual Property Rights – V. K. Ahuja
3. Intellectual Property Rights for Engineers – B. L. Wadhera

REFERENCE BOOKS

1. Intellectual Property Rights and the Law, Gogia Law Agency, by Dr. G.B. Reddy
2. Law relating to Intellectual Property, Universal Law Publishing Co, by Dr. B.L.Wadehra
3. IPR by P. Narayanan
4. Law of Intellectual Property, Asian Law House, Dr.S.R. Myneni.

Final Year (Semester-VII)

Digital Signal Processing Lab

BTEEV707	Digital Signal Processing Lab	LC13	0L- 0T - 2P	1 Credits
Teaching Scheme		Examination Scheme		
Practical: 02 hrs./week		Continuous Assessment: 30 Marks End Semester Exam: 20 Marks		

Digital Signal Processing Lab

(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Sample Experiments List:

1. Study of DSP software tools (MATLAB/Octave/Python/Scilab) and basic signal generation.
2. Generation and analysis of basic discrete-time signals (unit impulse, unit step, ramp, exponential, and sinusoidal signals).
3. Implementation of basic operations on discrete-time signals (time shifting, scaling, folding, and addition).
4. Implementation of linear convolution and verification using built-in functions.
5. Verification of the properties of convolution (commutative, associative, and distributive).
6. Computation of Z-transform and inverse Z-transform of discrete-time signals.
7. Solution of linear difference equations using the Z-transform.
8. Computation and analysis of DTFT and DFT of discrete-time signals.
9. Implementation of Fast Fourier Transform (FFT) using Radix-2 DIT and DIF algorithms.
10. Computation of linear convolution using the DFT method.
11. Design and realization of FIR digital filters using Rectangular, Hamming, Hanning, and Blackman window techniques.
12. Design and realization of IIR Butterworth digital filters using Impulse Invariance and Bilinear Transformation methods.
13. Implementation of multirate DSP techniques including decimation, interpolation, and sampling rate conversion.
14. Implementation of polyphase filters and digital filter banks.
15. Mini Project: Design and implementation of a DSP application such as audio filtering, speech enhancement, ECG signal filtering, or noise reduction.

Final Year (Semester-VII)

VLSI Verification & Testing Lab

BTEEV708	VLSI Verification & Testing Lab	LC14	0L- 0T - 2P	1 Credits
Teaching Scheme		Examination Scheme		
Practical: 02 hrs./week		Continuous Assessment: 30 Marks End Semester Exam: 20 Marks		

VLSI Verification & Testing Lab
(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Final Year (Semester-VII)

Analog VLSI Design Lab

BTEEV709	Analog VLSI Design Lab	LC15	0L- 0T - 2P	1 Credits
Teaching Scheme		Examination Scheme		
Practical: 02 hrs./week		Continuous Assessment: 30 Marks End Semester Exam: 20 Marks		

Analog VLSI Design Lab

(Minimum 8-10 experiments are to be performed based on contents from syllabus)

Final Year (Semester-VII) Project Work

BTEEV710	Project Work	PROJ	0L- 0T - 4P	2 Credits
Teaching Scheme		Examination Scheme		
Practical: 04 hrs./week		Continuous Assessment: 60 Marks End Semester Exam: 40 Marks		

Guidelines for Project

The students shall study in group of max. three members (or individual) on some special topic beyond the scope of the syllabus under the subjects of Electronics Engineering (VLSI Design & Technology). The selected topic may relate to VLSI design, semiconductor technology, electronics systems, embedded systems, IoT applications, FPGA-based systems, ASIC design, analog and digital electronics, hardware–software co-design, device modeling, signal processing, automation, EDA tools, verification methodologies, low-power systems, testing and reliability, System-on-Chip (SoC), nanoelectronics, and interdisciplinary applications involving electronics and software technologies. The work shall be carried out under the guidance of a faculty member by referring to current technical journals, conference proceedings, patents, standards, and reference books.

In this subject head, it is expected that the student should complete the following tasks.

1. Identify problem statement / idea which is solving one problem preferably local problem may be in their University / College / nearby vicinity.
2. Do the literature survey.
3. Design the solutions.
4. Implement solution using latest technology.
5. Write 50-60 pages report (use of latex is more suitable).
6. Present / demonstrate the solution in front of faculty members.

The students shall prepare the report and execution of project in the presence of guide and Panel Members/Examiner. The student is permitted to use audio-visual aids or any other such teaching aids.

Continues Assessment:

The Continues Assessment for this head will consists of the report written in a technical reporting manner and execution of project will be assessed by the internal examiner appointed by the HOD of concern department of the institution.

Final Year (Semester-VII)

Internship – IV (Evaluation) / MOOC

BTEEV711	Internship –IV (Evaluation) / MOOC	Internship	0L - 0T - 0P	AUDIT
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Internship –IV (Evaluation) / MOOC

Guidelines for Internships:

Guidelines for Field Training / Internship / Industrial Training:

1. To apply for a suitable Industrial Training, apply form to respective Organization concerned one semester before the Industrial Training Programmed commences.
2. Student can also apply through online platforms such as Internshala for industrial training.
3. Submit one copy of the offer letter for the Industrial Training to the Head of the department or Faculty coordinator (Industrial Training).
4. To complete the Industrial Training process within the specified time based on the Industrial Training Programme schedule.
5. Assessment within the Industrial Training context aims to evaluate the student's work quality and appropriateness to the field of study with reference to the learning outcomes of the Industrial Training Program.
6. Evaluation of the students' performance should be done in the next upcoming semester.
7. Those students who fails, they can also complete online certification courses which are available at free of cost on various MOOC platforms

Final Year (Semester-VIII)

Project Work / Internship

BTEEV801	Project Work / Internship	Project / Internship	0L- 0T - 24P	12 Credits
Teaching Scheme		Examination Scheme		
Practical: 24 hrs./week		Continuous Assessment: 60 Marks End Semester Exam: 40 Marks		

Guidelines for Project

The students shall study in group of max. three members (or individual) on some special topic beyond the scope of the syllabus under the subjects of Electronics Engineering (VLSI Design & Technology). The selected topic may relate to VLSI design, semiconductor technology, electronics systems, embedded systems, IoT applications, FPGA-based systems, ASIC design, analog and digital electronics, hardware–software co-design, device modeling, signal processing, automation, EDA tools, verification methodologies, low-power systems, testing and reliability, System-on-Chip (SoC), nanoelectronics, and interdisciplinary applications involving electronics and software technologies. The work shall be carried out under the guidance of a faculty member by referring to current technical journals, conference proceedings, patents, standards, and reference books.

In this subject head, it is expected that the student should complete the following tasks.

1. Identify problem statement / idea which is solving one problem preferably local problem may be in their University / College / nearby vicinity.
2. Do the literature survey
3. Design the solutions
4. Implement solution using latest technology
5. Write 60-70 pages report (use of latex is more suitable).
6. Present / demonstrate the solution in front of faculty member

The students shall prepare the report and execution of project in the presence of guide and Panel Members/examiner. The student is permitted to use audio-visual aids or any other such teaching aids.

Guidelines for Internships:

Guidelines for Field Training / Internship / Industrial Training:

1. To apply for a suitable Industrial Training, apply form to respective Organization concerned one semester before the Industrial Training Programmed commences.
2. Student can also apply through online platforms such as Internshala for industrial training.
3. Submit one copy of the offer letter for the Industrial Training to the Head of the department or Faculty coordinator (Industrial Training).

With effective from academic year 2024-25

4. To complete the Industrial Training process within the specified time based on the Industrial Training Programme schedule.
5. Assessment within the Industrial Training context aims to evaluate the student's work quality and appropriateness to the field of study with reference to the learning outcomes of the Industrial Training Program.
6. Evaluation of the students' performance should be done in the current semester as per instructions of university.

Continues Assessment:

The Continues Assessment for this head will consists of the report written in a technical reporting manner and execution of project/internship will be assessed by the internal examiner appointed by the HOD of concern department of the institution.