Dr. Babasaheb Ambedkar Technological University
(Established as a University of Technology in the State of Maharashtra)
(Under Maharashtra Act No. XXIX of 2014)
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Structure and Detailed Syllabus

for UG Degree

Minor in VLSI Design

in line with New Education Policy 2020

(Effective from Academic year 2025-26 for Affiliated Colleges Only)

Bucket for Minor in VLSI Design

Offered by

Electronics Engineering (VLSI Design & Technology)

Case I: B. Tech degree with Minor in VLSI Design (160-176 credits)

The Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with multidisciplinary minor (min.160-max.176 Credits) i.e. "**B. Tech in chosen Engg./ Tech. Discipline with Minor in VLSI Design**" (160-176 credits) enables students to take up four-six or required additional courses of 14 credits in the discipline other than **chosen Engg./ Tech. Discipline** distributed over semesters III to VIII.

Case II: Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with Double Minor (Multidisciplinary and Specialization Minor 180-194 credits)

The **Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with Double Minor** (Multidisciplinary and Specialization Minor, 180-194 credits), i.e. "**B. Tech in chosen Engg./ Tech. Discipline with minor in *other selected discipline in* Engineering (as MDM) with Specialization Minor in VLSI Design**" (180-194 credits) enables students to take up four-six additional courses of 14 credits in the discipline other than **chosen Engg./ Tech. Discipline** (for completion of multidisciplinary minor) and 18 to 20 extra credits in the **VLSI Design** distributed over semesters III to VIII. Here, the ***other selected discipline* in Engineering should be different from Specialization Minor i.e. VLSI Design**. This enables students to take up four-six or required additional courses of 18 to 20 credits in the discipline of **VLSI Design** distributed over semesters III to VIII, which are over and above the min.160-max.176 Credits. The decision regarding the mechanism of distribution of these 18-20 credits over semesters III to VIII, prescribed for the duration of four years will be taken by respective BoS. **Student must have CGPA equal to or greater than 7.5 at the end of second semester to go for this option**.

List of Courses for

Minor in VLSI Design

Sr. No.	Course Category	Course Code	Course Title	Teaching Scheme			Evaluation Scheme				Credit
				L	T	P	CA	MSE	ESE	Total	
1	SEM-III	25AF1378MD306	Digital System Design & Microprocessor	2	0	0	20	20	60	100	2
2	SEM-IV	25AF1378MD406	System Design using Verilog	2	0	0	20	20	60	100	2
3	SEM-V	25AF1378MD506	CMOS VLSI Design	4	0	0	20	20	60	100	3
4	SEM-VI	25AF1378MD605	Digital VLSI Design	2	0	0	20	20	60	100	3
5	SEM-VII	25AF1378MD705	Analog VLSI Design	2	0	0	20	20	60	100	2
6	SEM-VIII	25AF1378MD803	System Verilog	2	0	0	20	20	60	100	2
										600	**14**

Second Year (Semester –III)
Digital System Design & Microprocessor

25AF1378MD306	Digital System Design & Microprocessor	PCC	2L- 0T - 0P	2 Credits

Teaching Scheme	Examination Scheme
Lecture: 2 hrs./week	Continuous Assessment: 20 Marks Mid Semester Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is to:

1. To introduce fundamental digital concepts including number systems, binary codes, and the principles of Boolean algebra.
2. To teach systematic methods for simplifying Boolean functions using Karnaugh Maps and universal gates.
3. To design and analyze various standard combinational and sequential logic circuits.
4. To understand the architectural details, memory organization, and operating modes of the 8086 microprocessors.
5. To develop proficiency in 8086 assembly language programming, focusing on instruction sets and addressing modes.

Course Outcomes:

After completion of this course, students will be able to:

CO1. Convert between different number systems, represent signed and floating-point numbers, and apply Boolean algebra theorems to simplify expressions.

CO2. Minimize Boolean expressions for three, four, and five variables using K-Maps and implement them using NAND/NOR logic.

CO3. Design and explain the operation of common combinational circuits (e.g., adders, decoders) and sequential elements (e.g., flip-flops, counters, shift registers).

CO4. Describe 8086 architecture, memory segmentation, flag register, and differentiate between its minimum and maximum operating modes.

CO5. Write and analyze 8086 assembly language programs, utilizing various addressing modes and control flow instructions for arithmetic and branching operations.

Course Contents:

Unit 1: **[8 hours]**

Number systems and codes: Decimal, binary, octal and hexadecimal Number System, Number System conversions, Signed binary numbers: Sign Magnitude Approach, 1's complement Approach, and 2's Complement Approach, Binary codes: Weighted and Non-weighted codes, Alphanumeric codes, Reflective codes, digital logic gates, Boolean algebra, basic theorems & properties, Boolean functions, canonical and standard forms.

UNIT-2: **[8 hours]**

Gate level minimizations, K-Map – two variable, three variable, four variable and five variables, SOP, POS simplifications, NAND and NOR implementation and other two-level implementation.

UNIT-3: **[8 hours]**

Combinational circuits for code converters, Binary adders: half adder, full adder,N-bit parallel binary adder, Binary subtractor: half subtractor, full subtractor, N-bit Parallel Binary Subtractor, Binary Multiplier (2x2), comparator (1 and 2 bit only), decoder, encoder, priority encoder, multiplexers, demultiplexers

UNIT-4: **[8 hours]**

Memory Elements: latches and flipflops, Overview of clock.

Latches: SR latch, Gated SR latch, Gated D latch. Flip-flops: SR flip flop, JK flipflop, D flipflop, and T flipflop. Excitation Table for flip flops, flipflop conversion.

Counters: Asynchronous Counters: ripple, modulo, BCD or decade, and divide by N counter. Ring Counter, Twisted Tail Ring Counter.

Synchronous Counters**:** n-bit synchronous counter, synchronous counter as sequence generator.

Shift Registers.

UNIT-5: **[9 hours]**

Introduction to 8086 Microprocessor: Features, Architecture and Register Organization, Memory Organization & Segmentation, 8086 flag register, Signal description of 8086 common function signals, operating modes, Addressing Modes of 8086, Overview of various types of instruction set.

Textbooks:

1. John Wakerly, “Digital Design: Principles and Practices”, Pearson Education
2. D.V. Hall, “Digital Circuits and Systems”, Tata McGraw Hill, 1989
3. K M Bhurchandi, A K Ray, Advanced microprocessors and Peripherals, McGraw Hill Education India, 2012, 3rd ed.
4. Ramesh S. Gaonkar, "Microprocessor Architecture, Programming, and Applications with the 8085/8086", Penram International Publishing

Reference Books:

1. R.P. Jain, “Modern digital Electronics”, TataMcGrawHill,4thedition,2009.
2. Morris Mano and Michael Ciletti, “Digital Design”, Pearson Education
3. Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design”, McGraw-Hill Education

Second Year (Semester –IV)
System Design using Verilog

25AF1378MD406	System Design using Verilog	PCC	2L- 0T - 0P	2 Credits

Teaching Scheme	Examination Scheme
Lecture: 2 hrs./week	Continuous Assessment: 20 Marks Mid Sem Exam: 20 Marks End Semester Exam: 60 Marks

Course Objectives: The aim of this course is:

1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design.
2. To know the behavioural modelling of combinational and simple sequential circuits.
3. To know the behavioural modelling of algorithmic state machines.
4. To know the synthesis of combinational and sequential descriptions.
5. To know the architectural features of programmable logic devices.

Course Outcomes:

After completion of this course, students will be able to:

1. Demonstrate knowledge on HDL design flow, digital circuits design, switch de-bouncing, metastability, memory devices applications
2. Design and develop the combinational and sequential circuits using behavioural modelling
3. Solving algorithmic state machines using hardware description language
4. Analyse the process of synthesizing the combinational and sequential descriptions
5. Memorizing the advantages of programmable logic devices and their description in Verilog.

Course Contents:

Unit 1: **[8 hours]**

Introduction to Logic Design with Verilog: Structural models of combination logic, logic simulation, design verification, test methodology, propagation delay, truth table models of combinational and sequential logic with Verilog modules, ports, gate types, gate delays, dataflow modelling, continuous assignments delays, expressions, operators, operands, operator.

UNIT-2: **[8 hours]**

Logic Design with Behavioral Models of Combinational And Sequential Logic: Behavioral modeling, data types for behavioral modeling, behavioral models of combinational logic, propagation delay and continuous assignments, lathes and level sensitive circuits in Verilog, cyclic behavioral models of flip flops and latches, cyclic behavior and edge detection, a comparison of styles for behavioral modeling.

UNIT-3: **[8 hours]**

Behavioral models of multiplexers, encoders and decoders data flow model of a LFSR machines with multicycle operations, algorithmic state machine charts for behavioral modeling, asmd charts, behavioral models of counters, shift registers and register files, switch debounce, metastability, synchronizers for asynchronous signals.

UNIT-4: **[8 hour]**

Introduction to synthesis: synthesis of combinational logic, synthesis of sequential logic with latches, synthesis of three state devices and bus interfaces, synthesis of sequential logic with flip flops, synthesis of explicit state machines registered logic. Synchronous Counters: n-bit synchronous counter, synchronous counter as sequence generator.

UNIT-5: **[8 hours]**

Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.

Textbooks / Reference:

1. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009.
2. Samir Palnitkar - Verilog HDL, 2nd edition, Pearson Education, 2003.
3. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.
4. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.