Dr. Babasaheb Ambedkar Technological University
(Established as a University of Technology in the State of Maharashtra)
(Under Maharashtra Act No. XXIX of 2014)
P.O. Lonere, Dist. Raigad, Pin 402 103, Maharashtra
Telephone and Fax. 02140 - 275142
www.dbatu.ac.in

Structure and Detailed Syllabus

for UG Degree

Minor in VLSI Design & Technology

in line with New Education Policy 2020

(Effective from Academic year 2024-25 for main campus)

Bucket for Minor in VLSI Design & Technology

Case I: B. Tech degree with Minor in VLSI Design & Technology (160-176 credits)

The Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with multidisciplinary minor (min.160-max.176 Credits) i.e. "**B. Tech in chosen Engg./ Tech. Discipline with Minor in VLSI Design & Technology**" (160-176 credits) enables students to take up four-six or required additional courses of 14 credits in the discipline other than **chosen Engg./ Tech. Discipline** distributed over semesters III to VIII.

Case II: Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with Double Minor (Multidisciplinary and Specialization Minor 180-194 credits)

The **Bachelor's Engineering Degree in chosen Engg./ Tech. Discipline with Double Minor** (Multidisciplinary and Specialization Minor, 180-194 credits), i.e. "**B. Tech in chosen Engg./ Tech. Discipline with minor in *other selected discipline in* Engineering (as MDM) with Specialization Minor in VLSI Design & Technology**" (180-194 credits) enables students to take up four-six additional courses of 14 credits in the discipline other than **chosen Engg./ Tech. Discipline** (for completion of multidisciplinary minor) and 18 to 20 extra credits in the **VLSI Design & Technology** distributed over semesters III to VIII. Here, the ***other selected discipline* in Engineering should be different from Specialization Minor i.e. VLSI Design & Technology**. This enables students to take up four-six or required additional courses of 18 to 20 credits in the discipline of **VLSI Design & Technology** distributed over semesters III to VIII, which are over and above the min.160-max.176 Credits. The decision regarding the mechanism of distribution of these 18-20 credits over semesters III to VIII, prescribed for the duration of four years will be taken by respective BoS. **Student must have CGPA equal to or greater than 7.5 at the end of second semester to go for this option**.

Basic Semester wise credit distribution of the syllabus is as follows as per NEP-2020.

Semester		I	II	III	IV	V	VI	VII	VIII	Total Credits
Basic Science Course	BSC/ESC	06-08	08-10		--	--	--	--	--	14-18
Engineering Science Course		10-08	06-04		--	--	--	--	--	16-12
Programme Core Course (PCC)	Program Courses	--	02	08-10	08-10	10-12	08-10	04-06	04-06	44-56
Programme Elective Course (PEC)		--	--	--	--	04	08	02	06	20
Multidisciplinary Minor (MD M)	Multidisciplinary Courses		-	02	02	04	02	02	02	14
Open Elective (OE) Other than a particular program		--	--	04	02	02	--	--	--	08
Vocational and Skill Enhancement Course (VSEC)	Skill Courses	02	02	--	02	--	02	--	--	08
Ability Enhancement Course (AEC -01, AEC-02)	Humanities Social Science and Management (HSSM)	02	--	--	02	--	--	--	--	04
Entrepreneurship/Economics/ Management Courses		--		02	02	--	--	--	--	04
Indian Knowledge System (IKS)			02		--	--	--	--	--	02
Value Education Course (VEC)		--	--	02	02	--	--	--	--	04
Research Methodology	Experiential Learning Courses	--	--	--	--	--	--		04	04
Comm. Engg. Project (CEP)/Field Project (FP)		--	--	02	--	--	--	-	-	02
Project		--	--	--	--	--	--		04	04
Internship/ OJT		--	---			--	--	12	-	12
Co-curricular Courses (CC)	Liberal Learning Courses	02	02		--	--	--	--	-	04
Total Credits (Major)		**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**160-176**

List of Courses for

Minor in VLSI Design & Technology

Sr. No.	Course Name	Teaching Scheme	Duration (Weeks)	Credits	Institute Offering Course	Name of Professor/ Resource person	Link
1	VLSI Design	4Hrs/Week	8	2	IIT Bombay	Prof. A.N. Chandorkar	https://nptel.ac.in/courses/117101058
2	VLSI Data Conversion Circuits	4Hrs/Week	12	3	IIT Madras	Dr. Shanthi Pavan	https://nptel.ac.in/courses/117106034
3	VLSI Circuits	4Hrs/Week	12	3	IIT Madras	Prof. S. Srinivasan	https://nptel.ac.in/courses/117106092
4	VLSI Interconnects	4Hrs/Week	8	2	IIT Kharagpur	Prof. Sarang Pendharker	https://nptel.ac.in/courses/108105187
5	CMOS Digital VLSI Design	4Hrs/Week	8	2	IIT Roorkee	Prof. Sudeb Dasgupta	https://nptel.ac.in/courses/108107129
6	Analog VLSI Design	4Hrs/Week	12	3	IIT Kanpur	Prof. Imon Mondal	https://nptel.ac.in/courses/108104193
7	VLSI Signal Processing	4Hrs/Week	8	2	IIT Kharagpur	Prof. Mrityunjay Chakraborty	https://nptel.ac.in/courses/108105157
8	VLSI Design Flow: RTL to GDS	4Hrs/Week	12	3	IIIT Delhi	Prof. Sneh Saurabh	https://nptel.ac.in/courses/108106191
9	VLSI Design Verification and Test	4Hrs/Week	12	3	IIT Guwahati	Prof. Jatindra Kumar Deka, Dr. Santosh Biswas	https://nptel.ac.in/courses/106103016
10	Low Power VLSI Circuits & Systems	4Hrs/Week	8	2	IIT Kharagpur	Prof. Ajit Pal	https://nptel.ac.in/courses/106105034

Module-1 Introduction to VLSI Design

Module-2 Metal Oxide Seminconductor Field Effect Transistor (MOSFET)

Module-3 Fabrication Process and Layout Design Rules

Module-4 Propagation Delays in MOS

Module-5 Power Disipation in CMOS Circuits

Module-6 Semiconductor Memories

Module-7 I/O PADs

VLSI Data Conversion Circuits

1. Introduction to Data Conversion
2. Sampling-1
3. Sampling-2
4. Nonidealities in Samples
5. Noise due to Sampling
6. Distortion in a Sampling Switch
7. Gate Boosted Switches-1
8. Gate Boosted Switches-2
9. Charge Injection
10. S/H Characterization-1
11. S/H Characterization-2
12. FFTs and Leakage
13. Spectral Windows-1
14. Spectral Windows-2
15. ADC/DAC Definition
16. Quantization Noise-1
17. Quantization Noise-2
18. Over Sampling and Noise Shaping
19. Delta-Sigma Modulation-1
20. Delta-Sigma Modulation-2
21. Linearized Analysis
22. Stability of Delta Sigma Modulators
23. High Order DSMs
24. NTF Design and Tradeoffs
25. Single bit Modulators
26. Loop Filter Architectures
27. Continous-time Delta Sigma Modulation
28. Implicit Antialiasing
29. Modulators with NRZ and Impulsive DACs
30. High Order CTDSMs
31. CTDM Design
32. Excess Loop Delay (ELD)
33. ELD Compensation
34. Effect of Clock Jitter on CTDSMs-1
35. Effect of Clock Jitter on CTDSMs-2
36. Dynamic Range Scaling
37. Simulation of CTDSMs
38. Integrator Design-1
39. Integrator Design-2
40. Flash ADC Design
41. Latches and Metastability
42. Offset in a Latch-1
43. Offset in a Latch-2 Auto Zeroing
44. Auto Zeroing-2
45. Auto Zeroing-3
46. Auto Zeroing in flash ADCs
47. Flash ADCs Case Study
48. Flash ADC Case Study
49. Flash ADC in a Delta Sigma Loop
50. DAC Basics
51. Binary and Themometer DACs
52. Segmented DACs
53. Optimal DAC Segmentation
54. DAC Nonlinearities
55. Current Steering DACs-1
56. Current Steering DACs-2
57. DAC Mismatches in DSMs
58. Calibration and Randomization
59. Dynamic Element Matching-1
60. Dynamic Element Matching-2

VLSI Circuits

1. Introduction to VLSI Design
2. Combinational Circuit Design
3. Programmable Logic Devices
4. Programmable Array Logic
5. Review of Flip-Flops
6. Sequential Circuits
7. Sequential Circuit Design
8. MSI Implementation of Sequential Circuits
9. Design of Sequential Circuits using One Hot Controller
10. Verilog Modeling of Combinational Circuits
11. Modeling of Verilog Sequential Circuits - Core Statements
12. Modeling of Verilog Sequential Circuits - Core Statements(Contd)
13. RTL Coding Guidelines
14. Coding Organization - Complete Realization
15. Coding Organization - Complete Realization (Contd)
16. Writing a Test Bench
17. System Design using ASM Chart
18. Example of System Design using ASM Chart
19. Examples of System Design using Sequential Circuits
20. Examples of System Design using Sequential Circuits (Contd)
21. Microprogrammed Design
22. Microprogrammed Design (Continued)
23. Design Flow of VLSI Circuits
24. Simulation of Combinational Circuits
25. Simulation of Combinational and Sequential Circuits
26. Analysis of Waveforms using Modelsim
27. Analysis of Waveforms using Modelsim (Continued)
28. ModelSim Simulation Tool
29. Synthesis Tool
30. Synthesis Tool (Continued)
31. Synplify Tool - Schematic Circuit Diagram View
32. Technology View using Synplify Tool
33. Synopsys Full and Parallel Cases
34. Xilinx Place & Route Tool
35. Xilinx Place & Route Tool (Continued)
36. PCI Arbiter Design using ASM Chart
37. Design of Memories - ROM
38. Design of Memories- RAM
39. Design of External RAM
40. Design of Arithmetic Circuits
41. Design of Arithmetic Circuits (Continued)
42. Design of Arithmetic Circuits (Continued)
43. System Design Examples

44. System Design Examples (Continued)
45. System Design Examples (Continued)
46. System Design Examples (Continued)
47. System Design Examples (Continued)
48. System Design Examples using FPGA Board
49. System Design Examples using FPGA Board (Continued)
50. Advanced Features of Xilinx Project Navigator
51. System Design Examples using FPGA Board (Continued)
52. System Design Examples using FPGA Board (Continued)
53. System Design Examples using FPGA Board (Continued)
54. System Design Examples using FPGA Board (Continued)
55. Project Design Suggested for FPGA/ASIC Implementations

VLSI Interconnects

Week 1: Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Elmore delay in interconnects, Elmore delay in RC tree and branched interconnects

Week 2: Equivalent circuit of RC interconnect, Scaling Effects, Delay mitigation in RC interconnects, RC interconnect simulation session, Inductive effects in interconnects

Week 3: Distributed RLC Interconnect model (Frequency domain analysis), Transmission line equations. When to consider the inductive effects?, The transfer function of an interconnect, Time-domain response of a lumped model RLC circuit

Week 4: Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters.Simulation of RLC interconnects.Origin of the skin effect, Effective resistance at high frequencies

Week 5: Equivalent circuit to simulate skin effect, Power dissipation due to interconnects, Optimum interconnect width for minimizing total power dissipation. Heating effects and thermal modelling, Compact Thermal modeling with equivalent electrical circuit.

Week 6: Electromigration in interconnects, Mitigation of electromigration. Capacitive coupling in interconnects. Cross-talk and timing jitters in two identical interconnects. Effects of cross-talk and timing jitters.

Week 7: Techniques for mitigation of cross-talk.:23-erutceL Matrix formulation of coupled interconnects. Coupled RLC interconnects, Decoupling of interconnects by diagonalization of matrix , Analysis of coupled interconnects: Examples

Week 8: Analysis of coupled interconnects: Examples-2, Simulation of RC coupled interconnects, Extraction of capacitance (part-1), Extraction of capacitance (part-2), Extraction of inductance (part-1), Estimation of interconnect parameters from S parameters

CMOS Digital VLSI Design

Week 1 : L1: MOS Transistor Basic-I; L2: MOS Transistor Basic-I;
L3: MOS Transistor Basic-II; L4: MOS Parasitic & SPICE Model;
L5: CMOS Inverter Basics-I

Week 2 : L1: CMOS Inverter Basics-II; L2: CMOS Inverter Basics-III;
L3: Power Analysis-I; L4: Power Analysis-II;
L5: SPICE Simulation-I

Week 3 : L1: SPICE Simulation-II; L2: Combinational Logic Design-I; L3:
Combinational Logic Design-II; L4: Combinational Logic Design-III;
L5: Combinational Logic Design-IV

Week 4 : L1: Combinational Logic Design-V; L2: Combinational Logic Design-VI;
L3: Combinational Logic Design-VII; L4: Combinational Logic Design-VIII;
L5: Combinational Logic Design-IX

Week 5 : L1: Combinational Logic Design-X; L2: Logical Efforts-I;
L3: Logical EffortsII; L4: Logical Efforts-III;
L5: Sequential Logic Design-I

Week 6 : L1: Sequential Logic Design-II; L2: Sequential Logic Design-III;
L3:Sequential Logic Design-IV; L4: Sequential Logic Design-V;
L5: Sequential Logic Design-VI

Week 7 : L1: Sequential Logic Design-VII;
L2: Sequential Logic Design-VIII;
L3: Clocking Strategies for Sequential Design-I;
L4: Clocking Strategies for Sequential Design-II;
L5: Clocking Strategies for Sequential Design-III

Week 8 : L1: Clocking Strategies for Sequential Design-IV;
L2: Sequential Logic Design-IX;
L3: Clocking Strategies for Sequential Design-V;
L4: Concept of Memory & its Designing-I;
L5: Concept of Memory & its Designing-II

Analog VLSI Design

Week 1 & 2 : Introduction: Linearization of non-linear elements, Generation of small incremental linear equivalents from non-linear elements.

Week 3 & 4 : Basic amplifier design using MOSFET. Common source amplifier with resistive load.Biasing a common source amplifier. Gain limitations of the configuration.Introduction to swing limits. Relevance of the limitations in a integrated circuit.

Week 5 & 6 : Different biasing techniques of a common source amplifier. Use of negative feedback to realize stable biasing. Distinction between constant voltage and constant current biasing.

Week 7 & 8 : Introduction to controlled sources. Realizing controlled sources using a voltage controlled current source. Using MOSFETs to realize the controlled sources and other amplifier configurations. Body effects in an MOSFET. The effect of output resistance of a MOSFET on an amplifier configuration.

Week 9 & 10 : Introduction to active loads, and single stage differential amplifiers. Analysis of gain,swing limits, slew rate, common mode rejection ratio, power supply rejection ratio in a single stage differential amplifier.

Week 11 & 12 : Multi-stage amplifiers using controlled sources. Introduction of stability parameters of multistage amplifier when configured in negative feedback. Design and analysis of multi-stage amplifier by replacing the controlled sources with MOSFETs

VLSI Signal Processing

Week 1: Graphical representation of DSP algorithms, signal flow graph (SFG), data flow graph (DFG) and dependence graph (DG), high level transformation, critical path.

Week 2: Retiming of DFG, critical path minimization by retiming, loop retiming and iteration bound

Week 3: Cutset retiming, design of pipelined DSP architectures, examples

Week 4: Parallel realization of DSP algorithms, idea of unfolding, unfolding theorem, loop unfolding

Week 5: Polyphase decomposition of transfer functions, hardware efficient parallel realization of FIR filters, 2-parallel and 3-parallel filter architectures.

Week 6: Hardware minimization by folding, folding formula, examples from biquad digital filters,

Week 7: Delay optimization by folding, lifetime analysis, forward-backward data allocation, examples from digital filters

Week 8: Pipelining digital filters, look ahead techniques, clustered and scattered look ahead,combining parallel processing with pipelining in digital filters

VLSI Design Flow: RTL to GDS

Week 1: Basic Concepts of Integrated Circuit I: Structure, Fabrication,
Basic Concepts of Integrated Circuit II: Types, Design Styles, Designing vs. Fabrication,Economics, Figures of Merit
Overview of VLSI Design Flow I: Design Flows and Abstraction,
Overview of VLSI Design Flow II: Pre-RTL Methodology: Hardware/Software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis

Week 2: Overview of VLSI Design Flow III: RTL to GDS Implementation: Logic Synthesis
Overview of VLSI Design Flow IV: RTL to GDS Implementation: Physical Design
Overview of VLSI Design Flow V: Verification and Testing
Overview of VLSI Design Flow VI: Post-GDS Processes

Week 3: Hardware Modeling: Introduction to Verilog Simulation: Testbench,
Coverage Simulation: Events, Queues,
Mechanism of Simulation in Verilog RTL Synthesis: Verilog Constructs to Hardware

Week 4: Logic Optimization I: Definitions, Two-level logic optimization
Logic Optimization II: Multi-level logic optimization
Logic Optimization III: FSM Optimization
Formal Verification I: Introduction

Week 5: Formal Verification II: Formal Engines: BDD, SAT Solver
Formal Verification III: Combinational Equivalence Checking
Formal Verification IV: Model Checking
Technology Library: Delay and Power Models of Combinational and Sequential Cells

Week 6: Static Timing Analysis I: Synchronous Behavior, Timing Requirements;
Static Timing Analysis II: Timing Graph, Mechanism;
Static Timing Analysis III: Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations;
Constraints: Clock, I/O, Timing Exceptions

Week 7: Technology Mapping, Timing-driven Optimization, Power Analysis
Power-driven Optimization

Week 8: Design for Test I: Basics and Fault Models
Design for Test II: Scan Design Methodology
Design for Test III: ATPG
Design for Test IV: BIST

Week 9: Basic Concepts for Physical Design I: IC Fabrication, FEOL, BEOL;
Basic Concepts for Physical Design II: Interconnects and Parasitics;

Basic Concepts for Physical Design III: Signal Integrity;
Basic Concepts for Physical Design IV: Antenna Effect; Process-induced Variations; LEF files

Week 10: Chip Planning I: Partitioning;
Chip Planning II: Floorplanning: Die Size, I/O
Cells Chip Planning III: Floorplanning: Macros, Orientation, Pin Assignment
Chip Planning IV: Power Planning;

Week 11: Placement I: Global Placement, Wirelength Estimates
Placement II: Legalization, Detailed Placement, Timing-driven
Placement Placement III: Optimizations, Scan Cell Reordering; Spare Cell Placement
Clock Tree Synthesis I: Terminologies, Clock Distribution Networks, Clock Network Architectures

Week 12: Clock Tree Synthesis II: Routing, Useful Skews
Routing: Global and Detailed, Optimizations
Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off

VLSI Design Verification and Test

1. Scheduling, Allocation and Binding
2. Logic Optimization and Synthesis
3. Binary Decision Diagram
4. Temporal Logic
5. Model Checking
6. Introduction to Digital Testing
7. Fault Simulation and Testability Measures
8. Combinational Circuit Test Pattern Generation
9. Sequential Circuit Testing and Scan Chains
10. Built in Self test (BIST)

Low Power VLSI Circuits & Systems

1. Low Power VLSI Circuits & Systems

2. Introduction & Course Outline
3. MOS Transistors - I
4. MOS Transistors - II
5. MOS Transistors - III
6. MOS Transistors - IV
7. MOS Inverters - I
8. MOS Inverters - II
9. MOS Inverters - III
10. MOS Inverters - IV
11. Static CMOS Circuits - I
12. Static CMOS Circuits -II
13. MOS Dynamic Circuits -I
14. MOS Dynamic Circuits -II
15. Pass Transistor Logic Circuits - I
16. Pass Transistor Logic Circuits - II
17. MOS Memories
18. Finite State Machines
19. Switching Power Dissipation
20. Tutorial - I
21. Dynamic Power Dissipation
22. Leakage Power Dissipation
23. Supply Voltage Scaling - I
24. Supply Voltage Scaling - II
25. Supply Voltage Scaling - III
26. Supply Voltage Scaling - IV
27. Tutorial - II
28. Minimizing Switched Capacitance - I
29. Minimizing Switched Capacitance - II
30. Minimizing Switched Capacitance - III
31. Minimizing Switched Capacitance - IV
32. Minimizing Switched Capacitance - V
33. Minimizing Leakage Power - I
34. Minimizing Leakage Power - II
35. Minimizing Leakage Power - III
36. Variation Tolerant Design
37. Adiabatic Logic Circuits
38. Battery-Driven System Design
39. CAD Tools for Low Power
40. Tutorial – III
41. Course Summary