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(Established as a University of Technology in the State of Maharashtra)
(Under Maharashtra Act No. XXIX of 2014)
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B. Tech in VLSI Design & Technology

Structure and Detailed Syllabus

for

Major in VLSI Design & Technology In line with National Education Policy 2020

(Effective from Academic year 2024-25 for main campus)

Department of VLSI Design & Technology

Major in VLSI Design & Technology

The Bachelor's Engineering Degree with Honours in chosen Major Engg./ Tech. Discipline i.e. in VLSI Design & Technology with Major (180- 194 credits) enables students to take up five-six additional courses of 18 to 20 credits in the VLSI Design & Technology discipline distributed over semesters III to VIII. The decision regarding the mechanism of distribution of these 18-20 credits over semesters III to VIII, which are over and above the min.160-max.176 Credits prescribed for the duration of four years will be taken by Academic Authorities of University. Basic structure of the syllabus is as follows.

Semester		**I**	**II**	**III**	**IV**	**V**	**VI**	**VII**	**VIII**	**Total Credits**
Basic Science Course	BSC/ESC	06-08	08-10		--	--	--	--	--	14-18
Engineering Science Course		10-08	06-04		--	--	--	--	--	16-12
Programme Core Course (PCC)	Program Courses	--	02	08-10	08-10	10-12	08-10	04-06	04-06	44-56
Programme Elective Course (PEC)		--	--	--	--	04	08	02	06	20
Multidisciplinary Minor (MD M)	Multidisciplinary Courses		-	02	02	04	02	02	02	14
Open Elective (OE) Other than a particular program		--	--	04	02	02	--	--	--	08
Vocational and Skill Enhancement Course (VSEC)	Skill Courses	02	02	--	02	--	02	--	--	08
Ability Enhancement Course (AEC -01, AEC-02)	Humanities Social Science and Management (HSSM)	02	--	--	02	--	--	--	--	04
Entrepreneurship/Economics/ Management Courses		--		02	02	--	--	--	--	04
Indian Knowledge System (IKS)			02		--	--	--	--	--	02
Value Education Course (VEC)		--	--	02	02	--	--	--	--	04
Research Methodology	Experiential Learning Courses	--	--	--	--	--	--		04	04
Comm. Engg. Project (CEP)/Field Project (FP)		--	--	02	--	--	--	-	-	02
Project		--	--	--	--	--	--		04	04
Internship/ OJT		--	---			--	--	12	-	12
Co-curricular Courses (CC)	Liberal Learning Courses	02	02		--	--	--	--	-	04
Total Credits (Major)		**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**20-22**	**160-176**

List of Courses for

Major in VLSI Design & Technology

Students may take up to five-six additional courses of 18 to 20 credits in VLSI Design & Technology discipline distributed over semesters III to VIII for obtaining the major degree in VLSI Design & Technology.

Sr. No.	Course Name	Teaching Scheme	Duration (Weeks)	Credits	Institute Offering Course	Name of Professor/ Resource person	Link
1	Advanced VLSI design	4Hrs/Week	12	3	IIT Bombay	Prof. A. N. Chandorkar	https://archive.nptel.ac.in/courses/117/101/117101004/
2	Analog Electronic Circuits	4Hrs/Week	12	3	IIT Delhi	Prof. Shouribrata chatterjee	https://nptel.ac.in/courses/108102112
3	Electronic Systems Design: Hands on Circuits & PCB Design with CAD Software	4Hrs/Week	12	3	IIT Delhi	Prof. Ankur Gupta	https://nptel.ac.in/courses/108102481
4	Semiconductor Devices & Circuits	4Hrs/Week	12	3	IISc Bangalore	Prof. Sanjiv Sambandan	https://nptel.ac.in/courses/108108112
5	Digital VLSI Testing	4Hrs/Week	12	3	IIT Kharagpur	Prof. Santanu Chattopadhyay	https://nptel.ac.in/courses/117105137
6	VLSI Data Conversion Circuits	4Hrs/Week	12	3	IIT Madras	Dr. Shanti Pavan	https://nptel.ac.in/courses/117106034
7	VLSI Interconnects	4Hrs/Week	8	2	IIT Kharagpur	Prof. Sarang Pendharker	https://nptel.ac.in/courses/108105187
8	System Design through Verilog	4Hrs/Week	8	2	IIT Guwahati	Prof. Shaik Rafi Ahamed	https://nptel.ac.in/courses/108103179

1. Advanced VLSI Design

Module 1: CMOS VLSI Design for Power and Speed consideration
Historical Perspective and Future Trends in CMOS VLSI Circuit and System
Design- Part-I Historical Perspective and Future Trends in CMOS VLSI Circuit and System
Design - Part II Logical Effort - A way of Designing Fast CMOS Circuits Logical Effort - A way of Designing Fast CMOS
Circuits -Part II Logical Effort - A way of Designing Fast CMOS Circuits -Part III
Power Estimation and Control in CMOS VLSI circuits Power Estimation and Control in CMOS VLSI circuits -Part II Low Power Design Techniques- Part-I
Low Power Design Techniques -Part II

Module 2: Datapath Design Arithmetic Implementation Strategies for VLSI – Part I
Arithmetic Implementation Strategies for VLSI -Part II Arithmetic Implementation Strategies for VLSI -Part III Arithmetic Implementation Strategies for VLSI -Part IV

Module 3: Hardware Description Languages for VLSI Design
Managing concurrency and time in Hardware Description Languages, Introduction to VHDL Basic Components in VHDL, Structural Description in VHDL, Behavioural Description in VHDL Introduction to Verilog.

Module 4: FSM Controller/ Data path and processor Design
FSM + datapath (GCDexample), FSM + datapath (continued), Single Cycle MMIPS, Multicycle MMIPS, Multicycle MMIPS – FSM

Module 5: VLSI Design Automation
Brief Overview of Basic VLSI Design Automation Concepts, Netlist and System Partitioning Timing Analysis in the context of Physical Design Automation Engineering.

2. Analog Electronic Circuit

Week 1: Non-linear circuit analysis, diodes, load line concepts, introduction to the MOSFET
Week 2: DC operating point, biasing the MOSFET, small signal model of the MOSFET, small signal analysis
Week 3: Thevenin and Norton models, common source, common gate, common drain Circuits
Week 4: Source degenerated common source amplifier, cascode and cascaded circuits
Week 5: Current sources and current mirrors, biasing with current sources, constant gm Circuits
Week 6: Differential amplifiers, common mode and differential mode gains, CMRR, structure of a complete amplifier
Week 7: Folded cascode differential amplifier, self-biased active-load differential amplifier
Week 8: Feedback: examples of feedback amplifiers, current and voltage sensing, current and voltage feedback; op-amps and op-amp circuits
Week 9: High frequency model of the MOSFET, revision of common-gate, common-

source, common-drain circuits; poles and zeros in the transfer function.

Week 10: Poles and zeros of cascode amplifier, Miller theorem, phase margin, unity gain bandwidth, compensation of the cascaded amplifier

Week 11: Voltage regulators, LDOs, stability of regulators, power supply rejection, bandwidth.

Week 12: Power amplifiers, audio power amplifier, class-A/class-AB/class-B/class-C; push-pull class-AB power amplifier.

3. Electronic Systems Design: Hands on Circuits & PCB Design with CAD Software

Week 1:
Lecture 1: Introduction
Lecture 2: Passive circuit elements: R, L and C
Lecture 3: Resistor color coding, Surface mount capacitors and inductors on PCBs

Week 2:
Lecture 4: Active circuit elements: MOSFET, BJTs
Lecture 5: Network analysis: Kirchoff's Laws
Lecture 6: Network theorems: Thevenin, Norton, Maximum Power Transfer etc.

Week 3:
Lecture 7: Circuit Simulations using SPICE: Operating point analysis
Lecture 8: DC Simulations
Lecture 9: Small-Signal AC Simulations, Large Signal Simulations.

Week 4:
Lecture 10: Metal Interconnections, Through holes and vias.
Lecture 11: Interconnect design
Lecture 12: CMOS inverter basics

Week 5:
Lecture 13: CMOS inverter design
Lecture 14: Combinational circuit design: Part 1
Lecture 15: Combinational circuit design: Part 2

Week 6:
Lecture 16: Sequential circuit design: Part 1
Lecture 17: Sequential circuit design: Part 2
Lecture 18: Digital Design: Boolean Algebra

Week 7:
Lecture 19: Logic Families, Component Datasheets
Lecture 20: TTL/CMOS logic Interfacing Constraints
Lecture 21: Hardware Description Languages: VHDL and Verilog

Week 8:
Lecture 22: Digital circuit design: Inverters/Logic-gates.

Lecture 23: Digital circuit design: decoder/multiplexers.
Lecture 24: Digital circuit design: Adders/Multipliers and ALU.

Week 9:
Lecture 25: Understanding PCBs
Lecture 26: Single layer and multi-layer PCBs
Lecture 27: Holes, Vias, Layers Limitations

Week 10:
Lecture 28: Hands-on Training on PCB Prototyping-1
Lecture 29: Hands-on Training on PCB Prototyping-2
Lecture 30: Hands-on Training on PCB Prototyping-3

Week 11:
Lecture 31: Hands-on Training on PCB Prototyping-4
Lecture 32: Example: Basic PCB design 1
Lecture 33: Example: Basic PCB design 2

Week 12:
Lecture 34: Example: Advance PCB design 1
Lecture 35: Example: Advance PCB design 2
Lecture 36: Conclusion

4. Semiconductor Devices & Circuits

Week 1: Excursion in Quantum Mechanics
Week 2: Excursion in Solid State Physics
Week 3: Density of States, Fermi Function and Doping
Week 4: Recombination-Generation, Charge Transport and Continuity Equation
Week 5: Metal-Semiconductor (MS) Junctions
Week 6: PN Junctions
Week 7: Bipolar Junction Transistors (BJT)
Week 8: Metal Oxide Semiconductor Capacitors (MOSCAP) and CV Characteristics
Week 9: Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Week 10: MOSFET Continued
Week 11: Connections: Circuit Design to Device Physics
Week 12: Thin Film Transistors

5. Digital VLSI Testing

Week 1: Introduction: Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues

Week 2: Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture

Week 3: Design for Testability: Scan design rules, Scan design flow Fault Simulation: Introduction, Simulation models

Week 4: Fault Simulation: Logic simulation, Fault simulation

Week 5: Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms

Week 6: Test Generation: ATPG for non stuck-at faults, Other issues in test generation

Built-In-Self-Test: Introduction, BIST design rules

Week 7: Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures

Week 8: Test Compression: Introduction, Stimulus compression

Week 9: Test Compression: Stimulus compression, Response compression

Week 10: Memory Testing: Introduction, RAM fault models, RAM test generation

Week 11: Memory Testing: Memory BIST Power and Thermal Aware Test: Importance, Power models, Low power ATPG

Week 12: Power and Thermal Aware Test: Low power BIST, Thermal aware techniques

6. VLSI Conversion Circuits

(i) Introduction to A/D and D/A conversion:

sampling, quantization, quantization noise, aliasing and

reconstruction filtering.

(ii) ADC/DAC metrics: Differential and Integral

Nonlinearity, SNR, SNDR, SFDR and dynamic range.

(iii) ADC Architectures: Will cover two of these architectures in detail

(a) Flash and Floding ADCs.

(b) Oversampling Converters.

(c) Successive Approximation Converters.

(iv) DAC Design:

(a) Current steering DACs.

7. VLSI Interconnects

Week 1: Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Elmore delay in interconnects, Elmore delay in RC tree and branched interconnects

Week 2: Equivalent circuit of RC interconnect, Scaling Effects, Delay mitigation in RC interconnects, RC interconnect simulation session, Inductive effects in interconnects

Week 3: Distributed RLC Interconnect model (Frequency domain analysis), Transmission line equations. When to consider the inductive effects?, The transfer function of an interconnect, Time-domain response of a lumped model RLC circuit

Week 4: Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters. Simulation of RLC interconnects. Origin of the skin effect, Effective resistance at high frequencies

Week 5: Equivalent circuit to simulate skin effect, Power dissipation due to interconnects, Optimum interconnect width for minimizing total power dissipation. Heating effects and thermal modelling, Compact Thermal modeling with equivalent electrical circuit.

Week 6: Electromigration in interconnects, Mitigation of electromigration. Capacitive coupling in interconnects. Cross-talk and timing jitters in two identical interconnects. Effects of cross-talk and timing jitters.

Week 7: Techniques for mitigation of cross-talk. :23-erutceL Matrix formulation of coupled interconnects. Coupled RLC interconnects, Decoupling of interconnects by diagonalization of matrix, Analysis of coupled interconnects: Examples

Week 8: Analysis of coupled interconnects: Examples-2, Simulation of RC coupled interconnects, Extraction of capacitance (part-1), Extraction of capacitance (part-2), Extraction of inductance (part-1), Estimation of interconnect parameters from S parameters.

8. System Design Through Verilog

Week 1: Introduction to Verilog

Week 2: Gate level modelling

Week 3: Behavioral modelling I

Week 4: Behavioral modelling II

Week 5: Data flow modelling

Week 6: Switch level modelling

Week 7: Synthesis of combinational logic using Verilog

Week 8: Synthesis of sequential logic using Verilog