Id	1
Question	In 8085 microprocessor system with memory mapped I/O, which of the following is true?
A	Devices have 8-bit address line
B	Devices are accessed using IN and OUT instructions
C	There can be maximum of 256 input devices and 256 output devices
D	Arithmetic and logic operations can be directly performed with the I/O data
Marks	2
Unit	1

Id	2
Question	In the I/O mode, the 8255 ports work as
A	reset pins
B	set pins
C	programmable I/O ports
D	only output ports
Marks	2
Unit	3

Id	3
Question	In BSR mode, only port C can be used to
A	set individual ports
B	reset individual ports
C	set and reset individual ports
D	programmable I/O ports
Marks	2
Unit	3

Id	4
Question	The feature of mode 0 is
A	any port can be used as input or output
B	output ports are latched
C	maximum of 4 ports are available
D	all of the mentioned
Marks	2
Unit	3

Id	4
Question	The strobed input/output mode is another name of
A	mode 0

B	mode 1
C	mode 2
D	none
Marks	2
Unit	3

Id	5
Question	If the value of the pin STB (Strobe Input) falls to low level, then

A	input port is loaded into input latches
B	input port is loaded into output latches
C	output port is loaded into input latches
D	output port is loaded into output latches
Marks	2
Unit	3

Id	6
Question	The feature of mode 2 of 8255 is

A	single 8-bit port is available
B	both inputs and outputs are latched
C	port C is used for generating handshake signals
D	all of the mentioned
Marks	2
Unit	3

Id	7
Question	The number of hardware interrupts that the processor 8085 consists of is

A	1
B	3
C	5
D	7
Marks	2
Unit	3

Id	8
Question	The register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is
A	Interrupt Request Register
B	In-Service Register
C	Priority resolver
D	Interrupt Mask Register
Marks	2
Unit	3

Id	9
Question	The register that stores the bits required to mask the interrupt inputs is
A	In-service register
B	Priority resolver
C	Interrupt Mask register
D	None
Marks	2
Unit	3

Id	10
Question	The interrupt control logic

A	manages interrupts
B	manages interrupt acknowledge signals
C	accepts interrupt acknowledge signal
D	all of the mentioned
Marks	2
Unit	3

Id	11
Question	In a cascaded mode, the number of vectored interrupts provided by 8259A is
A	4
B	8
C	16
D	64
Marks	2
Unit	3

Id	12
Question	. When the PS(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
A	input to designate chip is master or slave
B	buffer enable
C	buffer disable
D	none
Marks	2
Unit	3

Id	13
Question	When non-specific EOI command is issued to 8259A it will automatically
A	set the ISR
B	reset the ISR
C	set the INTR
D	reset the INTR

Marks	2
Unit	3

Id	14
Question	In the application where all the interrupting devices are of equal priority, the mode used is
A	Automatic rotation
B	Automatic EOI mode
C	Specific rotation
D	EOI
Marks	2
Unit	3

Id	15
Question	The registers that store the keyboard and display modes and operations programmed by CPU are
A	I/O control and data buffers
B	Control and timing registers
C	Return buffers
D	Display address registers
Marks	2
Unit	3

Id	16
Question	The sensor RAM acts as 8-byte first-in-first-out RAM in
A	keyboard mode
B	strobed input mode
C	keyboard and strobed input mode
D	scanned sensor matrix mode
Marks	2
Unit	3

Id	17
Question	When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed in
A	scanned keyboard special error mode
B	scanned keyboard with N-key rollover
C	scanned keyboard mode with 2 key lockout
D	sensor matrix mode
Marks	2
Unit	3

Id	18
Question	Port C of 8255 can function independently as
A	input port
B	output port
C	either input or output ports
D	both input and output ports
Marks	2
Unit	3

Id	19
Question	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
A	data bus control
B	read logic control
C	control word register
D	none of the mentioned
Marks	2
Unit	3

Id	20
Question	The time taken by the ADC from the active edge of SOC(start of conversion) pulse till the active edge of EOC(end of conversion) signal is called
A	edge time
B	conversion time
C	conversion delay
D	time delay
Marks	2
Unit	4

Id	21
Question	The procedure of algorithm for interfacing ADC contain
A	ensuring stability of analog input
B	issuing start of conversion pulse to ADC
C	reading digital data output of ADC as equivalent digital output
D	all of the mentioned
Marks	2
Unit	4

Id	22
Question	When a key is pressed, the debounce circuit waits for 2 keyboard scans and then checks whether the key is still depressed in
A	scanned keyboard special error mode
B	scanned keyboard with N-key rollover
C	scanned keyboard mode with 2 key lockout
D	sensor matrix mode
Marks	2
Unit	3

Id	23
Question	The register that provides control and status information about serial port is
A	IP
B	IE
C	TSCON
D	PCON and SCON
Marks	2
Unit	3

Id	24
Question	A microcontroller at-least should consist of:
A	RAM, ROM, I/O devices, serial and parallel ports and timers
B	CPU, RAM, I/O devices, serial and parallel ports and timers
C	CPU, RAM, ROM, I/O devices, serial and parallel ports and timers
D	CPU, ROM, I/O devices and timers
Marks	2
Unit	5

Id	25
Question	Unlike microprocessors, microcontrollers make use of batteries because they have:
A	high power dissipation
B	low power consumption
C	low voltage consumption
D	low current consumption
Marks	2
Unit	5

Id	26
Question	How are microcontrollers classified on the basis of internal bus width?
A	8,16,32,64 bits
B	4,8,16,32 bits
C	8,16 bits
D	4,16,32 bits
Marks	2
Unit	5

Id	27
Question	What is the most appropriate criterion for choosing the right microcontroller of our choice?
A	speed
B	availability
C	ease with the product
D	all of the mentioned
Marks	2
Unit	5

Id	28
Question	When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?
A	PSW
B	SP
C	DPTR
D	PC
Marks	2
Unit	5

Id	29
Question	What is the file extension that is loaded in a microcontroller for executing any instruction?
A	.doc
B	.c
C	.txt
D	.hex
Marks	2
Unit	5

Id	30
Question	. Which architecture is followed by general purpose microprocessors?
A	Harvard architecture
B	Von Neumann architecture
C	None of the mentioned
D	All of the mentioned
Marks	2
Unit	5

Id	31
Question	Which architecture involves both the volatile and the non volatile memory?
A	Harvard architecture
B	Von Neumann architecture
C	None of the mentioned
D	All of the mentioned
Marks	2
Unit	5

Id	32
Question	Which architecture provides separate buses for program and data memory?
A	Harvard architecture
B	Von Neumann architecture
C	None of the mentioned
D	All of the mentioned
Marks	2
Unit	5

Id	33
Question	Which microcontroller doesn’t match with its architecture below?
A	Microchip PIC- Harvard
B	MSP430- Harvard
C	ARM7- Von Neumann
D	ARM9- Harvard
Marks	2
Unit	5

Id	34
Question	Harvard architecture allows:
A	separate program and data memory
B	pipe-ling
C	complex architecture
D	all of the mentioned
Marks	2
Unit	5

Id	35
Question	Which out of the following supports Harvard architecture?
A	ARM7
B	Pentium
C	SHARC
D	All of the mentioned
Marks	2
Unit	5

Id	36
Question	Why most of the DSPs use Harvard architecture?
A	they provide greater bandwidth
B	they provide more predictable bandwidth
C	they provide greater bandwidth & also more predictable bandwidth
D	none of the mentioned
Marks	2
Unit	5

Id	37

Question	Which of the following supports CISC as well as Harvard architecture?
A	ARM7
B	ARM9
C	SHARC
D	None of the mentioned
Marks	2
Unit	5

Id	38
Question	Which of the two architecture saves memory?
A	Harvard
B	Von Neumann
C	Harvard & Von Neumann
D	None of the mentioned
Marks	2
Unit	5

Id	39
Question	. 8051 series of microcontrollers are made by which of the following companies?

A	Atmel
B	Philips
C	Atmel & Philips
D	None of the mentioned
Marks	2
Unit	5

Id	40
Question	8051 series has how many 16 bit registers?
A	2
B	3

C	1
D	0
Marks	2
Unit	5

Id	41
Question	. When 8051 wakes up then 0x00 is loaded to which register?

A	DPTR
B	SP
C	PC
D	PSW
Marks	2
Unit	5

Id	42
Question	How are the bits of the register PSW affected if we select Bank2 of 8051?
A	PSW.5=0 and PSW.4=1
B	PSW.2=0 and PSW.3=1
C	PSW.3=1 and PSW.4=1
D	PSW.3=0 and PSW.4=1
Marks	2
Unit	5

Id	43
Question	. If we push data onto the stack then the stack pointer
A	increases with every push
B	decreases with every push
C	increases & decreases with every push
D	none of the mentioned
Marks	2
Unit	5

Id	44
Question	On power up, the 8051 uses which RAM locations for register R0- R7
A	00-2F
B	00-07
C	00-7F
D	00-0F
Marks	2
Unit	5

Id	45
Question	How many bytes of bit addressable memory is present in 8051 based microcontrollers?
A	8 bytes
B	32 bytes

C	16 bytes
D	128 bytes
Marks	C
Unit	5

Id	46
Question	. DJNZ R0, label is how many bit instructions?

A	2
B	3
C	1
D	Can’t be determined
Marks	2
Unit	5

Id	47
Question	JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register?
A	DPTR
B	B
C	A

D	PSW
Marks	2
Unit	5

Id	48
Question	When the call instruction is executed the topmost element of stack comes out to be
A	the address where stack pointer starts
B	the address next to the call instruction
C	address of the call instruction
D	next address of the stack pointer
Marks	2
Unit	5

Id	49
Question	LCALL instruction takes
A	2 bytes
B	4 bytes
C	3 bytes
D	1 byte
Marks	2
Unit	5

Id	50
Question	Are PUSH and POP instructions are a type of CALL instructions?
A	yes
B	no
C	none of the mentioned
D	cant be determined
Marks	2
Unit	5

Id	51
Question	What is the time taken by one machine cycle if crystal frequency is 20MHz?
A	1.085 micro seconds
B	0.60 micro seconds
C	0.75 micro seconds
D	1 micro seconds
Marks	2
Unit	5

Id	52
Question	What is the meaning of the instruction MOV A,05H?
A	data 05H is stored in the accumulator
B	fifth bit of accumulator is set to one
C	address 05H is stored in the accumulator
D	none of the mentioned
Marks	2
Unit	5

Id	53
Question	To initialize any port as an output port what value is to be given to it?
A	0xFF
B	0x00
C	0x01
D	A port is by default an output port
Marks	2
Unit	5

Id	54
Question	Which of the ports act as the 16 bit address lines for transferring data through it?
A	PORT 0 and PORT 1
B	PORT 1 and PORT 2
C	PORT 0 and PORT 2
D	PORT 1 and PORT 3
Marks	2
Unit	5

Id	55
Question	Which of the following registers are not bit addressable?
A	SCON
B	PCON
C	A
D	PSW
Marks	2
Unit	5

Id	56
Question	Which instruction is used to check the status of a single bit?
A	MOV A,P0
B	ADD A,#05H
C	JNB PO.0, label
D	CLR P0.05H
Marks	2
Unit	5

Id	57
Question	Which addressing mode is used in pushing or popping any element on or from the stack?
A	immediate
B	direct
C	indirect
D	register
Marks	2
Unit	5

Id	58
Question	What is the advantage of register indirect addressing mode?
A	it makes use of registers R0 and R1
B	it uses the data dynamically
C	it makes use of operator @
D	it is easy
Marks	2
Unit	5

Id	59
Question	Which of the following comes under the indexed addressing mode?
A	MOVX A, @DPTR
B	MOVC @A+DPTR,A
C	MOV A,R0
D	MOV @R0,A
Marks	2
Unit	5

Id	60
Question	Is this a valid statement? SETB A
A	yes
B	no
C	cant be determined
D	none of the mentioned
Marks	2
Unit	5

Id	61
Question	When we add two numbers the destination address must always be.
A	some immediate data
B	any register
C	accumulator
D	memory
Marks	2
Unit	5

Id	62
Question	DAA command adds 6 to the nibble if:
A	CY and AC are necessarily 1
B	either CY or AC is 1
C	no relation with CY or AC
D	CY is 1
Marks	2
Unit	5

Id	63
Question	If SUBB A,R4 is executed, then actually what operation is being applied?
A	R4+A
B	R4-A
C	A-R4
D	R4+A
Marks	2
Unit	5

Id	64
Question	A valid division instruction always makes:
A	CY=0,AC=1

B	CY=1,AC=1
C	CY=0,AC=0
D	no relation with AC and CY
Marks	2
Unit	5

Id	65

Question	In 8 bit signed number operations, OV flag is set to 1 if:
A	a carry is generated from D7 bit
B	a carry is generated from D3 bit
C	a carry is generated from D7 or D3 bit
D	a carry is generated from D7 or D6 bit
Marks	2
Unit	5

Id	66
Question	In unsigned number addition, the status of which bit is important?
A	OV
B	CY

C	AC
D	PSW
Answer	B
Marks	2
Unit	5

Id	67

Question	Which instructions have no effect on the flags of PSW?
A	ANL
B	ORL
C	XRL
D	All of the mentioned
Marks	2
Unit	5

Id	68
Question	ANL instruction is used _____
A	to AND the contents of the two registers
B	to mask the status of the bits
C	all of the mentioned
D	none of the mentioned
Marks	2
Unit	5

Id	69
Question	CJNE instruction makes _____
A	the pointer to jump if the values of the destination and the source address are equal
B	sets CY=1, if the contents of the destination register are greater then that of the source register
C	sets CY=0, if the contents of the destination register are smaller then that of the source register
D	none of the mentioned
Marks	2
Unit	5

Id	70
Question	XRL, ORL, ANL commands have _____

A	accumulator as the destination address and any register, memory or any immediate data as the source address
B	accumulator as the destination address and any immediate data as the source address
C	any register as the destination address and accumulator, memory or any immediate data as the source address
D	any register as the destination address and any immediate data as the source address
Marks	2
Unit	5

Id	71
Question	What is the clock source for the timers?
A	some external crystal applied to the micro-controller for executing the timer

B	from the crystal applied to the micro-controller
C	through the software
D	through programming
Marks	2
Unit	5

Id	72
Question	What is the frequency of the clock that is being used as the clock source for the timer?
A	some externally applied frequency f’
B	controller’s crystal frequency f
C	controller’s crystal frequency /12
D	externally applied frequency/12
Marks	2
Unit	5

Id	73
Question	What is the function of the TMOD register?
A	TMOD register is used to set different timer’s or counter’s to their appropriate modes
B	TMOD register is used to load the count of the timer
C	Is used to interrupt the timer
D	Is the destination or the final register where the result is obtained after the operation of the timer
Marks	2
Unit	5

Id	74
Question	What is the maximum delay that can be generated with the crystal frequency of 22MHz?
A	2978.9 sec
B	0.011 msec
C	11.63 sec
D	2.97 msec
Marks	2
Unit	5

Id	75
Question	Auto reload mode is allowed in which mode of the timer?
A	Mode 0
B	Mode 1
C	Mode 2
D	Mode 3
Marks	2
Unit	5

Id	76
Question	Find out the roll over value for the timer in Mode 0, Mode 1 and Mode 2?
A	00FFH,0FFFH,FFFFH
B	1FFFH,0FFFH,FFFFH
C	1FFFH,FFFFH,00FFH
D	1FFFH,00FFH,FFFFH

Marks	2
Unit	5

Id	77
Question	What steps are followed when we need to turn on any timer?
A	load the count, start the timer, keep monitoring it, stop the timer
B	load the TMOD register, load the count, start the timer, keep monitoring it, stop the

	timer
C	load the TMOD register, start the timer, load the count, keep monitoring it, stop the timer
D	none of the mentioned
Marks	2
Unit	5

Id	78
Question	If Timer 0 is to be used as a counter, then at what particular pin clock pulse need to be applied?
A	P3.3
B	P3.4
C	P3.5
D	P3.6
Marks	2
Unit	5

Id	79
Question	In the instruction “MOV TH1,#-3”, what is the value that is being loaded in the TH1 register?
A	0xFCH
B	0xFBH
C	0xFDH
D	0xFEH
Marks	2
Unit	5

Id	80
Question	TF1, TR1, TF0, TR0 bits are of which register?
A	TMOD
B	SCON
C	TCON
D	SMOD

Marks	2
Unit	5

Id	81
Question	Which devices are specifically being used for converting serial to parallel and from parallel to serial respectively?
A	timers
B	counters
C	registers
D	serial communication
Marks	2
Unit	5

Id	82
Question	What is the difference between UART and USART communication?
A	they are the names of the same particular thing, just the difference of A and S is there in it
B	one uses asynchronous means of communication and the other uses synchronous means of communication
C	one uses asynchronous means of communication and the other uses asynchronous and synchronous means of communication
D	one uses angular means of the communication and the other uses linear means of communication
Marks	2
Unit	5

Id	83
Question	Which of the following best describes the use of framing in asynchronous means of communication?
A	it binds the data properly
B	it tells us about the start and stops of the data to be transmitted or received
C	it is used for error checking
D	it is used for flow control
Marks	2
Unit	5

Id	84
Question	Which of the following signal control the flow of data?
A	RTS
B	DTR
C	RTS & DTR
D	None of the mentioned

Marks	2
Unit	5

Id	85
Question	Which of the following is the logic level understood by the micro-controller/micro-processor?
A	TTL logic level
B	RS232 logic level

C	None of the mentioned
D	TTL & RS232 logic level
Marks	2
Unit	5

Id	86
Question	What is a null modem connection?
A	no data transmission
B	no MAX232
C	the RxD of one is the TxD for the other
D	no serial communication
Marks	2
Unit	5

Id	87
Question	Which of the following best states the reason that why baud rate is mentioned in serial communication?
A	to know about the no of bits being transmitted per second
B	to make the two devices compatible with each other, so that the transmission becomes easy and error free
C	to use Timer 1
D	for wasting memory
Marks	2
Unit	5

Id	88
Question	With what frequency UART operates(where f denoted the crystal frequency)?
A	f/12
B	f/32
C	f/144
D	f/384
Marks	2
Unit	5

Id	89
Question	What is the function of the SCON register?
A	to control SBUF and SMOD registers
B	to program the start bit, stop bit, and data bits of framing
C	to control SMOD registers
D	none of the mentioned
Marks	2
Unit	5

Id	90
Question	What should be done if we want to double the baud rate?
A	change a bit of the TMOD register
B	change a bit of the PCON register
C	change a bit of the SCON register
D	change a bit of the SBUF register
Marks	2
Unit	5

Id	91
Question	When an interrupt is enabled, then where does the pointer moves immediately after this interrupt has occurred?
A	to the next instruction which is to be executed
B	to the first instruction of ISR
C	to the first location of the memory called the interrupt vector table
D	to the end of the program
Marks	2
Unit	5

Id	92
Question	What are the contents of the IE register, when the interrupt of the memory location 0x00 is caused?
A	0xFFH
B	0x00H
C	0x10H
D	0xF0H
Marks	2
Unit	5

Id	93
Question	After RETI instruction is executed then the pointer will move to which location in the program?
A	next interrupt of the interrupt vector table
B	next instruction of the program after the IE instruction
C	next instruction after the RETI in the memory
D	none of the mentioned
Marks	2
Unit	5

Id	94
Question	Which pin of the external hardware is said to exhibit INT0 interrupt?
A	pin no 10
B	pin no 11
C	pin no 12
D	pin no 13
Marks	2
Unit	5

Id	95
Question	Which bit of the IE register is used to enable TxD/RxD interrupt?
A	IE.D5
B	IE.D2
C	IE.D3
D	IE.D4
Marks	2
Unit	5

Id	96
Question	Which of the following combination is the best to enable the external hardware interrupt 0 of the IE register (assuming initially all bits of the IE register are zero)?
A	EX0=1
B	EA=1
C	any of the mentioned
D	EX0=1 & EA=1
Marks	2
Unit	5

Id	97
Question	Why normally LJMP instructions are the topmost lines of the ISR?

A	so as to jump to some other location where there is a wider space of memory available to write the codes
B	so as to avoid overwriting of other interrupt instructions
C	all of the mentioned
D	none of the mentioned
Marks	2
Unit	5

Id	98
Question	Which register is used to make the pulse a level or an edge triggered pulse?
A	TCON
B	IE

C	IPR
D	SCON
Marks	2
Unit	5

Id	99

Question	What is the disadvantage of a level triggered pulse?
A	a constant pulse is to be maintained for a greater span of time
B	difficult to analyze its effects
C	it is difficult to produce
D	another interrupt may be caused if the signal is still low before the completion of the last instruction
Marks	2
Unit	5

Id	100
Question	What is the correct order of priority that is set after a controller gets reset?
A	TxD/RxD > T1 > T0 >EX1 > EX0
B	TxD/RxD < T1 < T0<EX1 < EX0
C	EX0 > T0 > EX1 >T1> TxD/RxD
D	EX0 < T0 < EX1 < T1 < TxD/RxD
Marks	2
Unit	5

Id	101
Question	Which operator is the most important while assigning any instruction as register indirect instruction?
A	$
B	#
C	@
D	&
Marks	2
Unit	6

Id	102
Question	Find the number of times the following loop will be executed MOV R6,#200 BACK:MOV R5,#100 HERE:DJNZ R5, HERE DJNZ R6,BACK END
A	100
B	200
C	20000
D	2000
Marks	2
Unit	6

Id	103

Question	Calculate the jump code for again and here if code starts at 0000H
	MOV R1,#0
	MOV A,#0
	MOV R0,#25H
	AGAIN:ADD
	A,#0ECH
	JNC HERE
	HERE: INC R1
	DJNZ R0,AGAIN

	MOV R0,A END
A	F3,02
B	F9,01
C	E9,01
D	E3,02
Marks	2
Unit	6

Id	104
Question	How are the status of the carry, auxiliary carry and parity flag affected if the write

	instruction
	MOV A,#9C
	ADD A,#64H

A	CY=0,AC=0,P=0
B	CY=1,AC=1,P=0
C	CY=1,AC=1,P=1
D	CY=0,AC=1,P=0
Marks	2
Unit	6

Id	105
Question	How are the performance and the computer capability affected by increasing its internal bus width?
A	it increases and turns better
B	it decreases

C	remains the same
D	internal bus width doesn’t affect the performance in any way
Marks	2
Unit	5

Id	106
Question	3. What is the order decided by a processor or the CPU of a controller to execute an instruction?
A	decode,fetch,execute
B	execute,fetch,decode
C	fetch,execute,decode

D	fetch,decode,execute
Marks	2
Unit	6

Id	107

Question	Mov 09H,#05H;
	
	Mov A,# 11H;
	
	Mov R1 , # 09H;
	
	ADD A, 09H;
	
	XCHD A ,@ R1;

	DEC A after execution this instructions what will the contents of accumulator and @R1
A	14H, 05H
B	0EH, 06H
C	0FH, 05H
D	14H, 06H
Marks	2
Unit	6

Id	108

Question	MOV 20H, #20H;
	
	MOV A,#45H;
	
	MOV 21, #44H;

	MOV R0, #20H; XCHD A @R0 After execution of above program the content of accumulator, SP register and memory location 20H and 21H becomes
A	A=25H, SP=07H, memory location 20H=40H, memory location 21H=43H
B	A=25H, SP=07H, memory location 20H=40H, memory location 21H=44H
C	A=40H, SP=07H, memory location 20H=25H, memory location 21H=44H
D	None of the mentioned
Marks	2
Unit	6

Id	109
Question	Which instruction is used to check the status of a single bit?
A	MOV A,P0
B	ADD A,#05H
C	JNB PO.0, label
D	CLR P0.05H
Marks	2
Unit	6

Id	110

Question	MOV A, #09H;
	
	MOV R3, #09H;
	
	UP: RRA
	
	DJNZ R3 UP
	
	END
	
	After execution of the above program what will be the content of accumulator and how many times RRA instruction will be executed.

A	09H
B	42H
C	84H
D	12H
Marks	2

Unit	6

Id	111

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ANL A,#05H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	01H
C	None of the above
D	10H

Marks	2
Unit	6

Id	112

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV R3,08H
	
	LOOP: INC A
	
	DJNZ R3 LOOP
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	11H
B	0AH
C	0BH
D	0CH

Marks	2
Unit	6

Id	113

Question	If following program is executed then,What will be the content of accumulator?
	
	MOV A, #08H
	
	MOV R2, #05H
	
	ADD A, R2
	
	MOV DPTR, #2010H
	
	MOV @ DPTR,A

A	13H
B	0BH
C	2010
D	0DH
Marks	2
Unit	6

Id	114

Question	Mov 09H,#05H;
	
	Mov A,# 11H;
	
	Mov R1 , # 09H;
	
	ADD A, 09H;
	
	XCHD A ,@ R1;
	
	DEC A
	
	after execution this instructions what will the contents of accumulator and @R1

A	14H, 05H
B	0EH, 06H
C	0FH, 05H
D	14H, 06H
Marks	2

Unit	6

Id	115

Question	MOV 20H, #20H;
	
	MOV A,#45H;
	
	MOV 21, #44H;
	
	MOV R0, #20H;
	
	XCHD A @R0
	
	After execution of above program the content of accumulator, SP register and memory location 20H and 21H becomes

A	A=25H, SP=07H, memory location 20H=40H, memory location 21H=43H
B	A=25H, SP=07H, memory location 20H=40H, memory location 21H=44H
C	A=40H, SP=07H, memory location 20H=25H, memory location 21H=44H
D	None of the mentioned
Marks	2

Unit	6

Id	116
Question	Which instruction is used to check the status of a single bit?
A	MOV A,P0
B	ADD A,#05H
C	JNB PO.0, label
D	CLR P0.05H
Marks	2
Unit	6

Id	117

Question	MOV A, #09H;
	
	MOV R3, #09H;
	
	UP: RRA
	
	DJNZ R3 UP
	
	END
	
	After execution of the above program what will be the content of accumulator and how many times RRA instruction will be executed.

A	09H
B	42H
C	84H
D	12H
Marks	2
Unit	6

Id	118

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ANL A,#05H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	01H
C	None of the above
D	10H
Marks	2
Unit	6

Id	119

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV R3,08H
	
	LOOP: INC A
	
	DJNZ R3 LOOP
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	11H
B	0AH
C	0BH
D	0CH
Marks	2
Unit	6

Id	120

Question	If following program is executed then,What will be the content of accumulator?
	
	MOV A, #08H
	
	MOV R2, #05H
	
	ADD A, R2
	
	MOV DPTR, #2010H
	
	MOV @ DPTR,A

A	13H
B	0BH
C	2010
D	0DH
Marks	2
Unit	6

Id	121
Question	Which of the following are correct
A	ARM, AVR, PIC and 8051 are families of Microcontroller
B	AVR Stands for Advanced Virtual RISC
C	Microcontrollers are either RISC or CISC kind of instruction architecture and ARM stands for Advanced RISC Machines
D	all of the above are correct
Marks	2
Unit	5

Id	122

Question	What will be content of A, after the following set of instructions are executed?
	
	MOV @R0, #04H
	MOV A, #11H
	XCHD A, @R0

A	40H
B	14H
C	41H
D	01H
Marks	2
Unit	6

Id	123
Question	Find the number of times the following loop will be executed MOV R6,#200 BACK: MOV R5,#100 HERE: DJNZ R5, HERE DJNZ R6, BACK END
A	infinite times the loop will executed.
B	2000 times the loop will executed.
C	20000 times the loop will executed.
D	all of the above are correct
Marks	2
Unit	6

Id	124

Question	Mov 09H,#05H;
	
	Mov A,# 11H;
	
	Mov R1 , # 09H;
	
	ADD A, 09H;
	
	XCHD A ,@ R1;
	
	DEC A
	
	after execution this instructions what will the contents of accumulator and @R1

A	14H, 05H
B	0EH, 06H
C	0FH, 05H
D	14H, 06H
Marks	2
Unit	6

Id	125

Question	MOV 20H, #20H;
	
	MOV A,#45H;
	
	MOV 21, #44H;
	
	MOV R0, #20H;
	
	XCHD A @R0
	
	After execution of above program the content of accumulator, SP register and memory location 20H and 21H becomes

A	A=25H, SP=07H, memory location 20H=40H, memory location 21H=43H
B	A=25H, SP=07H, memory location 20H=40H, memory location 21H=44H
C	A=40H, SP=07H, memory location 20H=25H, memory location 21H=44H
D	None of the mentioned
Marks	2
Unit	6

Id	126
Question	Which instruction is used to check the status of a single bit?
A	MOV A,P0
B	ADD A,#05H
C	JNB PO.0, label
D	CLR P0.05H
Marks	2
Unit	6

Id	127

Question	MOV A, #09H;
	
	MOV R3, #09H;
	
	UP: RRA
	
	DJNZ R3 UP
	
	END
	
	After execution of the above program what will be the content of accumulator and how many times RRA instruction will be executed.

A	09H
B	42H
C	84H
D	12H
Marks	2
Unit	6

Id	128

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ANL A,#05H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	01H
C	None of the above
D	10H
Marks	2
Unit	6

Id	129

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV R3,08H
	
	LOOP: INC A
	
	DJNZ R3 LOOP
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	11H
B	0AH
C	0BH
D	0CH
Marks	2
Unit	6

Id	130

Question	If following program is executed then,What will be the content of accumulator?
	
	MOV A, #08H
	
	MOV R2, #05H
	
	ADD A, R2
	
	MOV DPTR, #2010H
	
	MOV @ DPTR,A

A	13H
B	0BH
C	2010

D	0DH
Marks	2
Unit	6

Id	131
Question	Which of the following are correct
A	ARM, AVR, PIC and 8051 are families of Microcontroller
B	AVR Stands for Advanced Virtual RISC
C	Microcontrollers are either RISC or CISC kind of instruction architecture and ARM stands for Advanced RISC Machines

D	all of the above are correct
Marks	2
Unit	5

Id	132

Question	What will be content of A, after the following set of instructions are executed?
	
	MOV @R0, #04H
	MOV A, #11H
	XCHD A, @R0

A	40H
B	14H
C	41H
D	01H
Marks	2
Unit	6

Id	133
Question	Find the number of times the following loop will be executed MOV R6,#200 BACK: MOV R5,#100 HERE: DJNZ R5, HERE DJNZ R6, BACK END
A	infinite times the loop will executed.
B	2000 times the loop will executed.
C	20000 times the loop will executed.
D	all of the above are correct

Marks	2
Unit	6

Id	134

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ORL A,#55H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	20H
C	01h
D	none of the above
Marks	2

Unit	6

Id	135

Question	Mov 10H, #10H;
	
	Mov A, #25H;
	
	Mov 11,#24H;
	
	Mov R0,#10H;
	
	XRL A @R0
	
	ADD A, #04H
	
	After execution of the this program, what will be the contents of accumulater?

A	35H
B	39H
C	29H
D	None of the answer correct
Marks	2

Unit	6

Id	136

Question	MOV A, #56H
	
	MOV R1, #50H
	
	MOV 50H, # 45H
	
	XCHD A, @R1
	
	What is the result at A, R1?

A	55H, 50H
B	55H, 46H
C	46H, 50H
D	46H, 55H
Marks	2
Unit	6

Id	137

Question	Mov 10H, #15H;
	
	Mov A, #25H;
	
	Mov 11,#24H;
	
	Mov R0,#10H;
	
	XRL A @R0
	
	ADD A, #04H
	
	After execution of the this program, what will be the contents of accumulater?

A	CFH
B	34H
C	D3H
D	some instructions are wrong content of A will be 00h
Marks	2
Unit	6

Id	138

Question	What will be the content of A after execution of the following program?
	Mov A, #55H
	
	Mov R3, #10
	
	Mov R2, #70
	
	CPL, A
	
	RR A
	
	ADD A R2
	
	END

A	55H
B	00H
C	C5H
D	AAH
Marks	2
Unit	6

Id	139

Question	Mov 09H,#05H;
	
	Mov A,# 11H;
	
	Mov R1 , # 09H;
	
	ADD A, 09H;
	
	XCHD A ,@ R1;
	
	DEC A
	
	after execution this instructions what will the contents of accumulator and @R1

A	14H, 05H
B	0EH, 06H
C	0FH, 05H
D	14H, 06H
Marks	2
Unit	6

Id	140

Question	MOV 20H, #20H;
	
	MOV A,#45H;
	
	MOV 21, #44H;
	
	MOV R0, #20H;
	
	XCHD A @R0
	
	After execution of above program the content of accumulator, SP register and memory location 20H and 21H becomes

A	A=25H, SP=07H, memory location 20H=40H, memory location 21H=43H
B	A=25H, SP=07H, memory location 20H=40H, memory location 21H=44H
C	A=40H, SP=07H, memory location 20H=25H, memory location 21H=44H
D	None of the mentioned
Marks	2
Unit	6

Id	141
Question	Which instruction is used to check the status of a single bit?
A	MOV A,P0
B	ADD A,#05H
C	JNB PO.0, label
D	CLR P0.05H
Marks	2
Unit	6

Id	142

Question	MOV A, #09H;
	
	MOV R3, #09H;
	
	UP: RRA
	
	DJNZ R3 UP
	
	END
	
	After execution of the above program what will be the content of accumulator and how many times RRA instruction will be executed.

A	09H
B	42H
C	84H
D	12H
Marks	2
Unit	6

Id	143

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ANL A,#05H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	01H
C	None of the above
D	10H
Marks	2
Unit	6

Id	144

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV R3,08H
	
	LOOP: INC A
	
	DJNZ R3 LOOP
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	11H
B	0AH
C	0BH
D	0CH
Marks	2
Unit	6

Id	145

Question	If following program is executed then,What will be the content of accumulator?
	
	MOV A, #08H
	
	MOV R2, #05H
	
	ADD A, R2
	
	MOV DPTR, #2010H
	
	MOV @ DPTR,A

A	13H
B	0BH
C	2010
D	0DH
Marks	2
Unit	6

Id	146
Question	Which of the following are correct
A	ARM, AVR, PIC and 8051 are families of Microcontroller
B	AVR Stands for Advanced Virtual RISC
C	Microcontrollers are either RISC or CISC kind of instruction architecture and ARM stands for Advanced RISC Machines
D	all of the above are correct
Marks	2
Unit	5

Id	147

Question	What will be content of A, after the following set of instructions are executed?
	
	MOV @R0, #04H
	MOV A, #11H
	XCHD A, @R0

A	40H
B	14H
C	41H
D	01H
Marks	2
Unit	6

Id	148
Question	Find the number of times the following loop will be executed MOV R6,#200 BACK: MOV R5,#100 HERE: DJNZ R5, HERE DJNZ R6, BACK END
A	infinite times the loop will executed.
B	2000 times the loop will executed.
C	20000 times the loop will executed.
D	all of the above are correct
Marks	2
Unit	6

Id	149

Question	MOV A,#03H
	
	MOV R1,#06H
	
	MOV 06H,#08H
	
	ADD A,@R1
	
	ORL A,#55H
	
	END
	
	What will be the content of accumulator after execution of this instructions??

A	0BH
B	20H
C	01h
D	none of the above
Marks	2
Unit	6

Id	150

Question	Mov 10H, #10H;
	
	Mov A, #25H;
	
	Mov 11,#24H;
	
	Mov R0,#10H;
	
	XRL A @R0
	
	ADD A, #04H
	
	After execution of the this program, what will be the contents of accumulater?

A	35H
B	39H
C	29H
D	None of the answer correct
Marks	2
Unit	6

Id	151

Question	MOV A, #56H
	
	MOV R1, #50H
	
	MOV 50H, # 45H
	
	XCHD A, @R1
	
	What is the result at A, R1?

A	55H, 50H
B	55H, 46H
C	46H, 50H
D	46H, 55H
Marks	2
Unit	6

Id	152

Question	Mov 10H, #15H;
	
	Mov A, #25H;
	
	Mov 11,#24H;
	
	Mov R0,#10H;
	
	XRL A @R0
	
	ADD A, #04H
	
	After execution of the this program, what will be the contents of accumulater?

A	CFH
B	34H
C	D3H
D	some instructions are wrong content of A will be 00h
Marks	2
Unit	6

Id	153
Question	What will be the content of A after execution of the following program? Mov A, #55H

	Mov R3, #10
	
	Mov R2, #70
	
	CPL, A
	
	RR A
	
	ADD A R2
	
	END

A	55H
B	00H
C	C5H
D	AAH
Marks	2
Unit	6