DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY
LONERE – RAIGAD -402 103
End Semester Examination

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Branch: B. Tech.(Group A/Group B) **Sem.:- I**
Subject with Subject Code:- Basic Electronics Engineering (EXE105)
Date:- **Marks: 60** **Time:- 3 Hr.**

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Instructions:-

1. Attempt any ***five*** questions.
2. All questions carry equal marks.
3. Illustrate your answer with neat sketches, diagrams etc. wherever necessary.
4. Necessary data is given in the respective questions. If such data is not given, it means that the knowledge of that component is a part of examination.
5. If some part or parameter is noticed to be missing, you may appropriately assume and state it clearly in the answer-book.

Q.1. A] Describe essential features of the following bonds: 06
Solution: 2 marks each for correct description with diagram of
(a) Ionic bond b) Covalent bond c) Metallic bond

B] Discuss the classification of materials with electrical engineering point of view. 06
Solution: 2 marks each for correct description with diagram of Insulator, Semiconductor and Conductor

Q.2. Attempt any ***two*** of the followings:

A] How does the Fermi level changes with increasing temperature in the extrinsic semiconductors (***n***- type and ***p*** -type)? Sketch the energy level diagram. 06
Solution: For each; ***n-type and p-type*** description along with energy level diagram: 03 marks each.

B] What is Hall effect? Calculate Hall voltage, Hall coefficient and Hall angle. 06
Solution: Definition: 01 marks; Calculation of Hall Voltage: 02 marks; Hall cofficent:02 marks and Hall ange:01 Marks.

C] Find the built-in voltage for a ***Si*** P-N junction with $N_A = 10^{15} c\,m^{-3}$ 06
and $N_D = 10^{17} c\,m^{-3}$ at room temperature with $n_i = 10^{10} c\,m^{-3}$.

SOL:

$$V_{bi} = \frac{kT}{q} . \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

At room temperature, $T \approx 300\,K$,

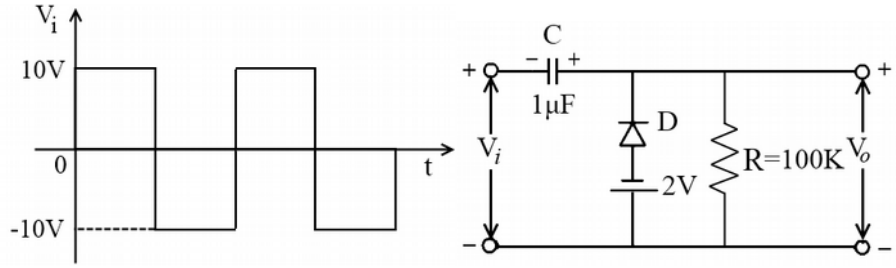
$$kT \approx 0.026\,eV$$

$$\left(\frac{kT}{q}\right) = 0.026\,V$$

$$\therefore V_{bi} = 0.026 \times \ln\left(\frac{10^{17} \times 10^{15}}{10^{10}}\right)$$

$$\therefore V_{bi} = 0.718\,V$$

Q.3 A] Sketch V_o for the circuit and the input shown. D is a silicone diode with cut in voltage $V_v = 0.6V$. 06



Solution:

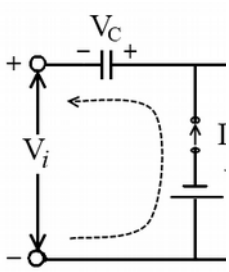
1. In the negative half cycle of input, D will be on and it will charge the capacitor with the polarities shown in figure

$$\therefore V_i - V_R - V_v - V_C = 0$$

$$\therefore V_C = V_i - V_R - V_v$$

$$= 10 - 2 - 0.6$$

$$\therefore V_C = 7.4\,Volts$$



2. Output voltage $V_o = V_i + V_C$

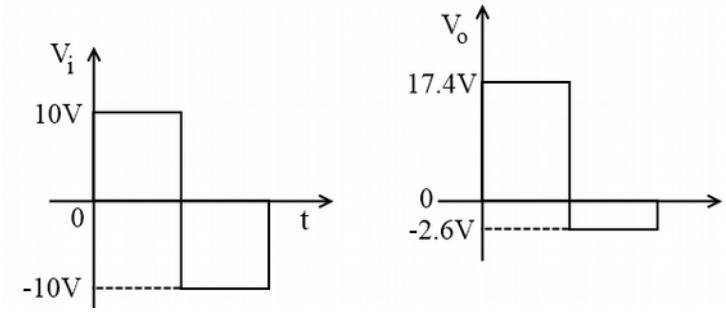
$\therefore$ In the positive half cycle,

$V_o = 10 + 7.4 = 17.4\,V$

And in the negative half cycle,

$V_o = -10 + 7.4 = -2.6\,V$

The input output waveforms are shown in figure.



B] Write a note on depletion layer capacitance and diffusion capacitance. 06

Solution: Correct description along with diagram 03 marks each.

Q.4 Define transistor biasing. List and explain different transistor biasing techniques with suitable diagrams and expressions. 12

Solution:

- ✓ Definition : 02 mark;
- ✓ Explanation with diagrams and equations for: fixed bias (03 marks), collector bias (03 marks) and voltage divider bias (04marks).

Q.5. Attempt any ***two*** of the followings:

A] Describe the working of center tap full wave rectifier with neat diagram and waveforms. Explain: Peak inverse voltage, ripple factor and efficiency with respect to a center tap full wave rectifier. 06

Solution:

- ✓ Working with circuit diagram:03 marks
- ✓ Explanation of Peak inverse voltage, ripple factor and efficiency: 01 mark each.

B] Explain different types of resistors in detail. 06

Solution:

- ✓ Diagram and description of each resistor: 5 marks.
- ✓ Calculation of 1KΩ color code: 01 mark

C] Describe construction and working of a LVDT. State any two advantages and disadvantages of LVDT. 06

Solution:

- Diagram and description of construction and working 02 marks each.
- Ant two Advantages and disadvantages of LVDT: 01 mark each

Q.6 A] Do as directed: 06

a) Obtain 2's complement of 10111011 **(01 mark)**

Solution:

```
  10111011
+        1
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  10111100
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b) Add $(AF1.B3)_H + (FFF.E)_H$ **(02 mark)**

Solution :

(AF1.B3)16 = (101011110001.10110011)2 and

(FFF.E)16 =11111111111.1110)2 can also be written as (111111111111.11100000)2 to have the same number of bits in the integer and fractional parts. The two numbers can now be added as follows:

```
0101011110001.10110011
0111111111111.11100000
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1101011110001.10010011
```

c) Determine the floating point representation of $(-142)_{10}$ using IEEE single precision format. **(03 mark)**

Solution:

As a first step, the binary equivalent of $(142)_{10}$ need to be calculated as $(142)_{10} = (10001110)2$.

- $(10001110)2 = 1.000\ 1110 \times 2^7 = 1.0001110e + 0111$.
- The mantissa = 0001110 00000000 00000000.
- The exponent = 00000111.
- The biased exponent = 00000111 + 01111111 = 10000110.
- The sign of the mantissa = 1.
- Therefore, (−142)10 = 11000011 00001110 00000000 00000000.

B] Explain AND, OR, NAND,NOR, Ex-OR, Ex-NOR logic gates with their logic diagram and truth table. 06

Solution: Logic diagram and truth table of a gate: **01 mark each**

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