DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,
LONERE – RAIGAD -402 103
Mid Semester Examination – October - 2017

Branch:M.Tech. (VLSI) **Sem.:- I**

Subject with Subject Code:- Basics of VLSI (MTVLC103) **Marks: 20**

Date:- **Time:- 1 Hr.**

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Instructions:-

(Marks)

Q.No.1 **Attempt any one of the following** **(08)**

a) With the help of equations describe behavior of MOS Transistors in cut-off, linear and saturation region. Also draw I-V Characteristics of NMOS.

ANS: **Refer Fig2.7, Page no.45, Author: Neil weste , Title: CMOS VLSI Design**

Refer 2.2, page no. 42 Author: Neil weste , Title: CMOS VLSI Design

b)Design CMOS gate for the following Function:

i) F1= $\overline{(A+B+C).D}$

ANS: **Refer Fig1.18, Page no.12, Author: Neil weste , Title: CMOS VLSI Design**

ii) F2= $\overline{AB+DE+C}$

Similarly design it

Q.No. 2 **Attempt any three of the following:** **(12)**

a) Draw and explain VLSI Design Flow.

ANS: **Refer -1.6, Fig1.48, Page no.28, Author: Neil Weste , Title: CMOS VLSI Design**

b) Explain Latches in CMOS.

ANS: **Refer -1.4.9, Page no.16, Author: Neil Weste , Title: CMOS VLSI Design**

c) Define Noise margin. Explain low noise and high noise margin with Transfer characteristics of CMOS Inverter.

ANS: **Refer -2.5.3, Fig2.27, Fig2.28 Page no.62, Author: Neil Weste , Title: CMOS VLSI Design**

d) Describe following Non-ideal IV effects

i) Velocity saturation ii) Mobility degradation

iii) Junction Leakage iv) Subthreshold conduction

ANS: **Refer -2.4, 2.4.1, 2.4.4, 2.4.5 , Page no.51, Author: Neil Weste , Title: CMOS VLSI Design**