DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,
LONERE – RAIGAD -402 103
Mid Semester Examination – October - 2017

Branch:M.Tech (VLSI) **Sem.:- I**

Subject with Subject Code:- MTVLC102 **Marks: 20**

Date:- 09-10-17 **Time:- 1 Hr.**

(Marks)

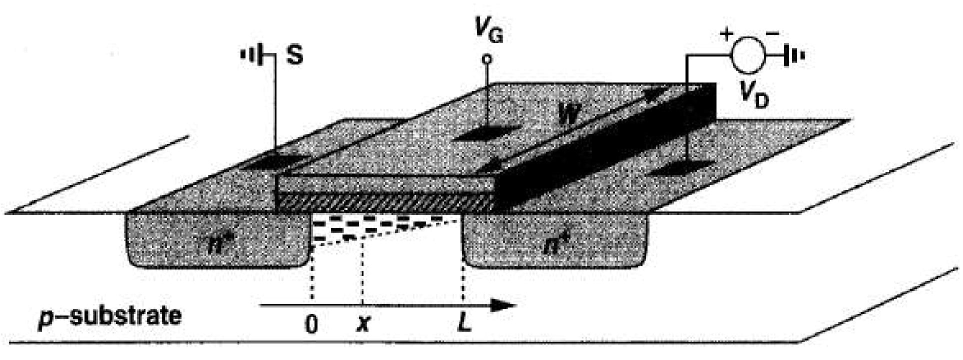
Q.No.1 Attempt any one of the following (08)

a.) Derive the equation for drain current in NMOS. Also draw the I/V characteristic.

Ans. 1)a) Consider a semiconductor bar carrying a current I. If the charge density along the direction of current is Qd coulombs per meter and the velocity of the charge is v meters per second, then

$$I = Qd \cdot v$$

Consider an NMOS whose source and drain are connected to ground as shown in fig below.



Assuming the onset of inversion occurs at $V_{GS} = V_{TH}$, the inversion charge density produced by the gate oxide capacitance is proportional to $V_{GS} - V_{TH}$.

For $V_{GS} \geq V_{TH}$. any charge placed on the gate must be mirrored by the charge in the channel, yielding a uniform channel charge density (charge per unit length) equal to

$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$

where WCox to represent the total capacitance per unit length
Since the channel potential varies from zero at the source to V_D at the drain, the local voltage difference between the gate and the channel varies from V_G to V_G - V_D. Thus, the charge density at a point x along the channel can be written as

$$Q_d(x) = WCox[V_{GS} - V(x) - V_{TH}]$$

where V (x) is the channel potential at x.

the current is given by

$$I_D = -WCox[V_{GS} - V(x) - V_{TH}]v$$

where the negative sign indicate the charge carriers are negative and v denotes the velocity of the electrons in the channel.
For semiconductors, v = μE, where μ, is the mobility of charge carriers and E is the electric field.
Therefore, E(x) = -dV /dx and representing the mobility of electrons by μ_n, we have

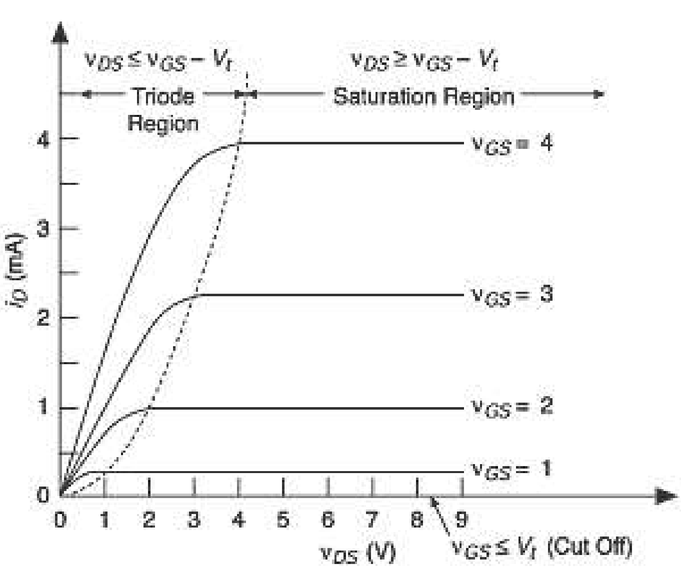
$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

subject to boundary conditions V(O) = 0 and V(L) = V_{DS}.
Multiplying both sides by dV and performing integration, we obtain

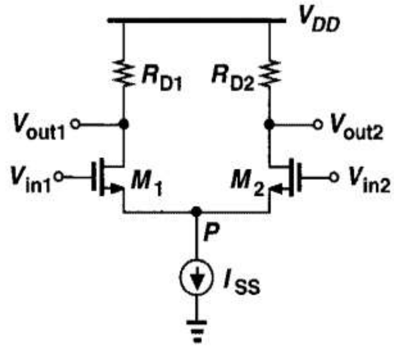
$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]dV$$

Since I_D is constant along the channel,

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$



b.) Derive the differential output current for the figure shown below assuming the circuit is symmetric, M1 and M2 are saturated, and λ = 0



Ans. 1)b) For the differential pair

$$V_{out1} = V_{DD} - R_{D1} \cdot I_{D1} \text{ and}$$

$$V_{out2} = V_{DD} - R_{D2} \cdot I_{D2}$$

i.e. $V_{out1} - V_{out2} = R_{D2} \cdot I_{D2} - R_{D1} \cdot I_{D1} = R_D \,(I_{D2} - I_{D1})$ …..if $R_{D2} = R_{D1} = R_D$

Assuming the circuit is symmetric, M_1 and M_2 are saturated, and $\lambda = 0$.
Since the voltage at node P is equal to $V_{in1} - V_{GS1}$ and $V_{in2} - V_{GS2}$,

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

For a square-law device, we have,

$$(V_{GS} - V_{TH})^2 = \frac{I_D}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}}$$

and, therefore,

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} + V_{TH}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}$$

Squaring the both the sides of above eq. and recognizing that $I_{D1} + I_{D2} = I_{SS}$, we obtain

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}} (I_{SS} - 2\sqrt{I_{D1} I_{D2}})$$

That is,

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}}$$

Squaring the two sides again and noting that,

$$4(I_{D1} \cdot I_{D2}) = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I^2_{SS} - (I_{D1} - I_{D2})^2$$

We obtain,

$$(I_{D1} - I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1} - V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2$$

Thus,

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

Q.No. 2 Attempt any three of the following: (12)

a.) Explain Body effect in MOSFET

Ans 2)a) Body Effect:

Since the S and D junctions remain reverse-biased, it is surmise that the device continues to operate properly but certain characteristics may change.

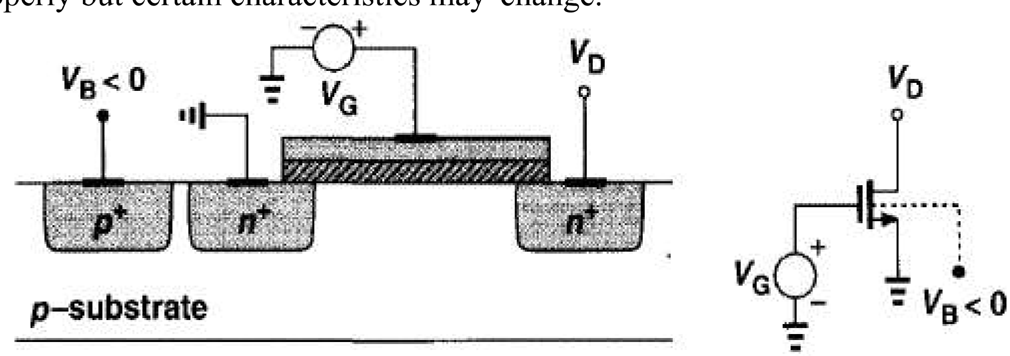
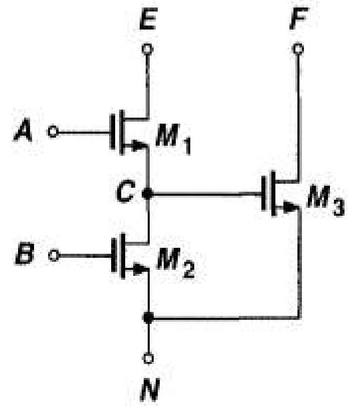


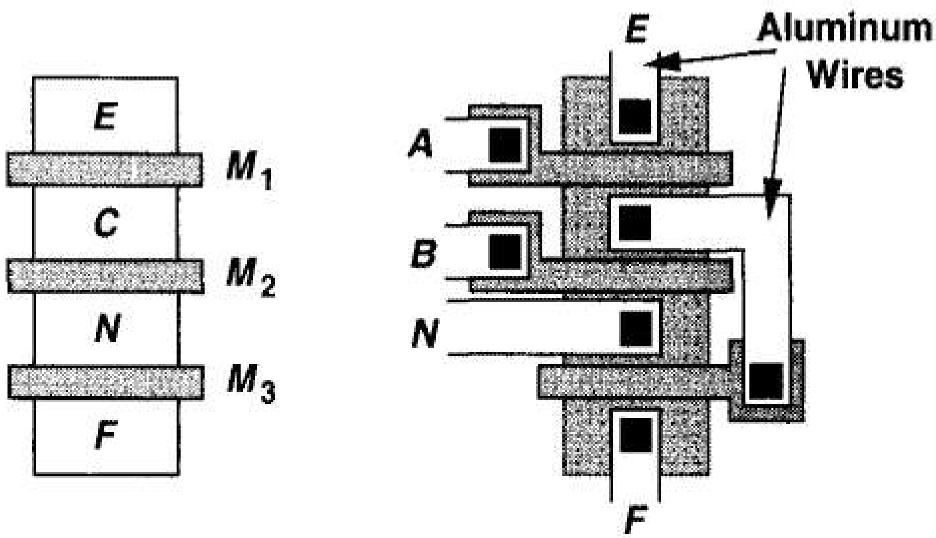
Figure : NMOS device with negative bulk voltage

To understand the effect, suppose $V_S = V_D = 0$, and V_G is somewhat less than VTH so that a depletion region is formed under the gate but no inversion layer exists. As V_B becomes more negative, more holes are attracted to the substrate connection, leaving a larger negative charge behind, i.e, the depletion region becomes wider. Also the threshold voltage is a function of the total charge in the depletion region because the gate charge must mirror Qd before an inversion layer is formed. Thus, as V_B drops and Q_d increases, V_{TH} also increases. This is called the "body effect" or the "backgate effect."

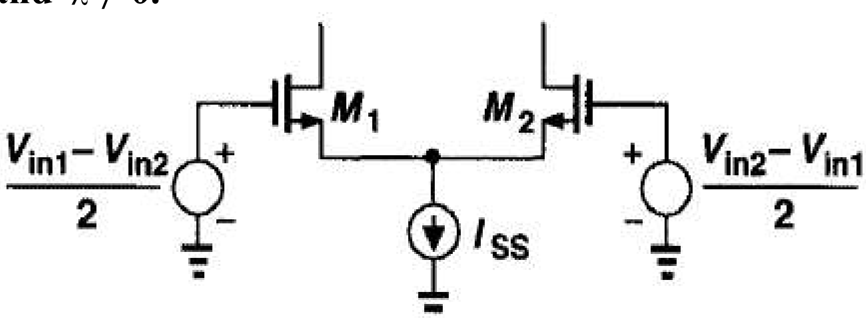
b.) Draw the layout of the circuit shown in Fig



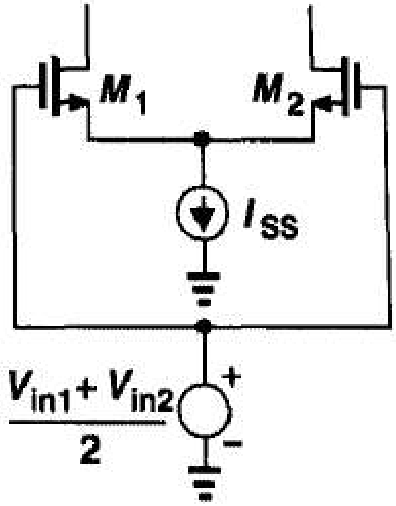
Ans 2)b)



c.) In the circuit of shown below, calculate Vx and Vy if $V_{in1} \neq -V_{in2}$ and $\lambda \neq 0$.



Ans 2)c) Simpliying the given circuit,



For differential-mode operation, from the above circuit we have,

$$V_X = -g_m(R_D \| r_{O1})\frac{V_{in1} - V_{in2}}{2}$$
$$V_Y = -g_m(R_D \| r_{O2})\frac{V_{in2} - V_{in1}}{2}.$$

$$V_X - V_Y = -g_m(R_D \| r_O)(V_{in1} - V_{in2}),$$

d.) Explain advantage of current mirror.

Ans 2)d) The advantages of a current mirror are:

1. low input impedance makes the input current insensitive to the output impedance of the input source
2. high output impedance makes the output current insensitive to the impedance of the output load
3. inversion of sources to sinks or sinks to sources
4. accurate gain
5. shifts between different power rails.