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LONERE – RAIGAD -402 103

Mid Semester Examination – October - 2017

Branch: M.Tech (VLSI and Embedded System Design) **Sem.:- I**

Subject with Subject Code:- Advanced Embedded Logic (MTVEC103) **Marks: 20**

Date:- **Time:- 1 Hr.**

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Q1 a) What are the different CPU modes of ARM? State its significance.

Modes can switch modes due to external events (interrupts) or programmatically.

- User mode: The only non-privileged mode.
- FIQ mode: A privileged mode that is entered whenever the processor accepts a Fast interrupt request.
- IRQ mode: A privileged mode that is entered whenever the processor accepts an interrupt.
- Supervisor (svc) mode: A privileged mode entered whenever the CPU is reset or when an SVC instruction is executed.
- Abort mode: A privileged mode that is entered whenever a prefetch abort or data abort exception occurs.
- Undefined mode: A privileged mode that is entered whenever an undefined instruction exception occurs.
- System mode (ARMv4 and above): The only privileged mode that is not entered by an exception. It can only be entered by executing an instruction that explicitly writes to the mode bits of the CPSR.
- Monitor mode (ARMv6 and ARMv7 Security Extensions, ARMv8 EL3): A monitor mode is introduced to support TrustZone extension in ARM cores.
- Hyp mode (ARMv7 Virtualization Extensions, ARMv8 EL2): A hypervisor mode that supports Popek and Goldberg virtualization requirements for the non-secure operation of the CPU.
- Thread mode (ARMv6-M, ARMv7-M, ARMv8-M): A mode which can be specified as either privileged or unprivileged, while whether Main Stack Pointer (MSP) or Process Stack Pointer (PSP) is used can also be specified in CONTROL register with privileged access. This mode is designed for user tasks in RTOS environment but it's typically used in bare-metal for super-loop.
- Handler mode (ARMv6-M, ARMv7-M, ARMv8-M): A mode dedicated for exception handling (except the RESET which are handled in Thread mode). Handler mode always uses MSP and works in privileged level.

Any 8 modes each of 1 mark.

Q1 b) What are the different features of 32 bit ARM as a RISC architecture?

The 32-bit ARM architecture includes the following RISC features:

- Load/store architecture.
- No support for unaligned memory accesses in the original version of the architecture. ARMv6 and later, except some microcontroller versions, support unaligned accesses for half-word and single-word load/store instructions with some limitations, such as no guaranteed atomicity.
- Uniform 16× 32-bit register file (including the program counter, stack pointer and the link register).
- Fixed instruction width of 32 bits to ease decoding and pipelining, at the cost of decreased code density. Later, the Thumb instruction set added 16-bit instructions and increased code density. Mostly single clock-cycle execution.
- Conditional execution of most instructions reduces branch overhead and compensates for the lack of a branch predictor.
- Arithmetic instructions alter condition codes only when desired.
- 32-bit barrel shifter can be used without performance penalty with most arithmetic instructions and address calculations.
- Have powerful indexed addressing modes.
- A link register supports fast leaf function calls.
- A simple, but fast, 2-priority-level interrupt subsystem has switched register banks.

Any 8 features each of 1 mark.

Q2 a) State the bit wise significance of Current Program Status Register of ARM?

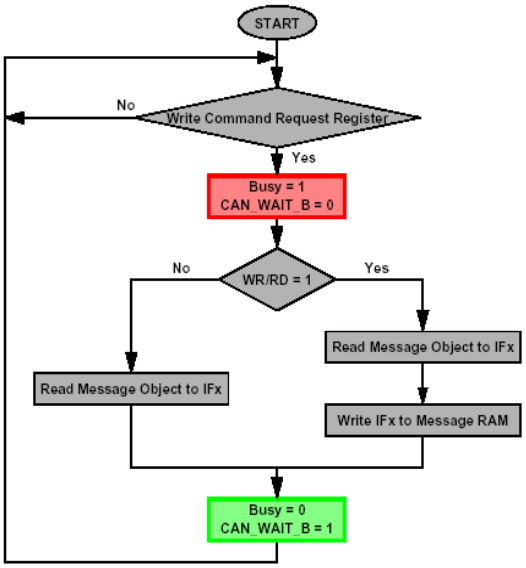
Current Program Status Register (CPSR) has the following 32 bits.

- M (bits 0–4) is the processor mode bits.
- T (bit 5) is the Thumb state bit.
- F (bit 6) is the FIQ disable bit.
- I (bit 7) is the IRQ disable bit.
- A (bit 8) is the imprecise data abort disable bit.
- E (bit 9) is the data endianness bit.
- IT (bits 10–15 and 25–26) is the if-then state bits.
- GE (bits 16–19) is the greater-than-or-equal-to bits.
- DNM (bits 20–23) is the do not modify bits.
- J (bit 24) is the Java state bit.
- Q (bit 27) is the sticky overflow bit.
- V (bit 28) is the overflow bit.
- C (bit 29) is the carry/borrow/extend bit.
- Z (bit 30) is the zero bit.
- N (bit 31) is the negative/less than bit.

Full bit structure should give 4 marks.

Q2 b) What is the process of sending a message using CAN protocol?

- At each CAN device, the start of frame bit notifies a transmission is being sent.
- The identifier bit shows the priority of the message along with determining which device the data belongs to.



Discussion of all the steps as in above flow diagram= 2 marks and flow diagram 2 marks

Q2 c) Interface ARM with RS232C? Assume any suitable device.

Interfacing diagram 2 marks.

Discussion 2 marks.

Q2 d) Interface ARM with I2C device? Assume any suitable device.

Interfacing diagram 2 marks.

Discussion 2 marks.