DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,

LONERE – RAIGAD -402 103

Mid Semester Examination – October - 2017

Branch: M.Tech (VLSI and Embedded System Design) Sem.:- I

Subject with Subject Code:- VLSI Technology and Design (MTVEC101)

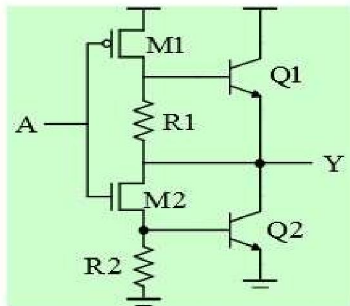
Marks: 20

Date:- Time:- 1 Hr.

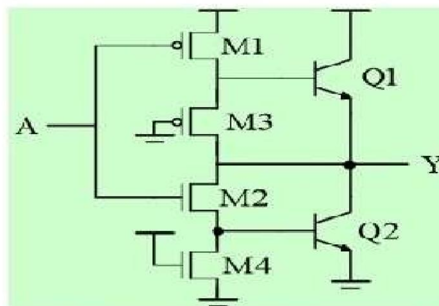
Q1 a) Enlist different types of bi-cmos inverter.

The following figures show BiCMOS inverter of various types.

Resistive shunt type and active shunt type:

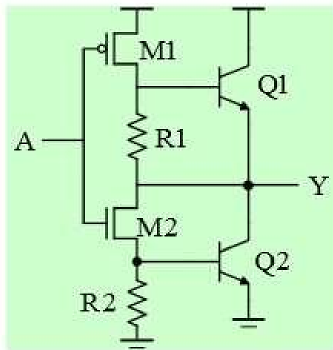


R-Type BiCMOS

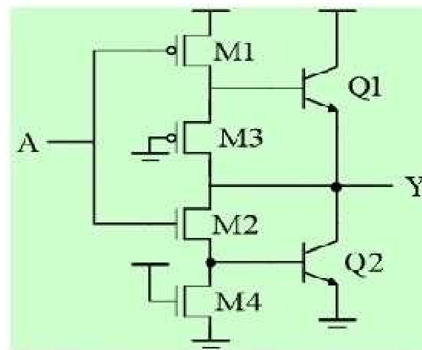


R-Type Active BiCMOS

Simple R-type BiCMOS inverter and R-type active BiCMOS inverter types:

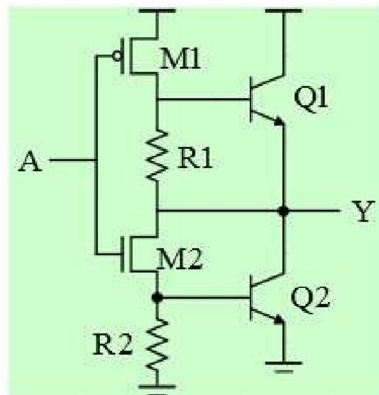


R-Type BiCMOS

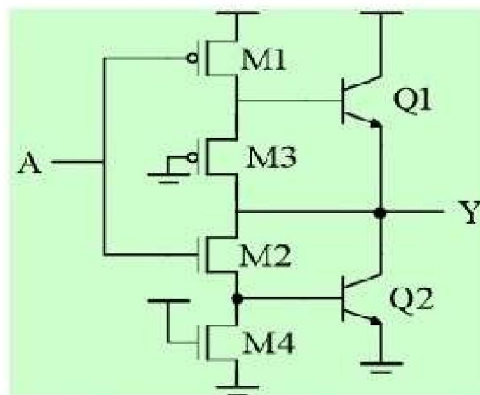


R-Type Active BiCMOS

Feedback type BiCMOS and parallel output CMOS(collector emitter shunting) type of inverters:



R-Type BiCMOS

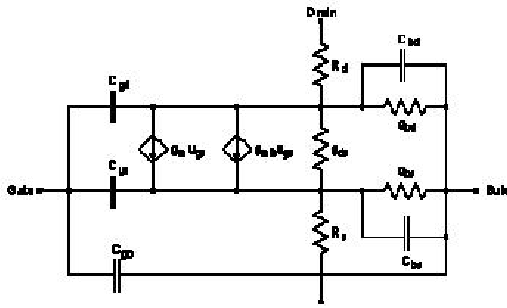


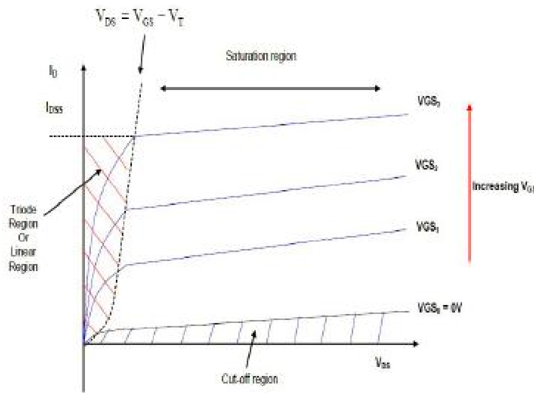
R-Type Active BiCMOS

Any 4 type each of 1 mark and description 2 marks.

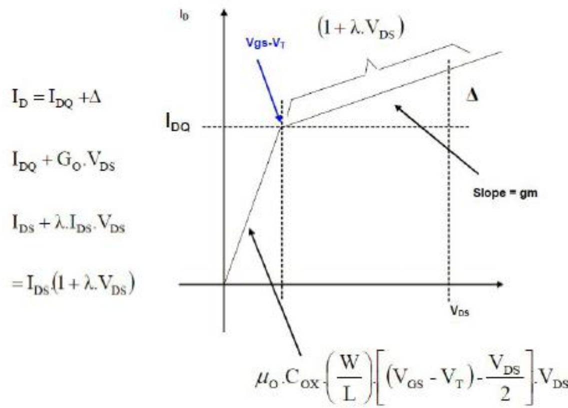
Q1 b) Derive the drain current equation in saturation region of MOS with the use of MOS transistor circuit model.

MOS transistor circuit model and characteristics:





Drain current analysis in various region:



$$ID = \mu_O.C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)-\frac{V_{DS}}{2}\right].V_{DS}(1+\lambda.V_{DS})$$

Where μ_O = Surface mobility of device

$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$ = capacitance per unit area of gate oxide

W = Effective channel width

L = Effective channel length

W/L = Known as the aspect ratio

VT = Device threshold voltage

λ = Channel length modulation parameter

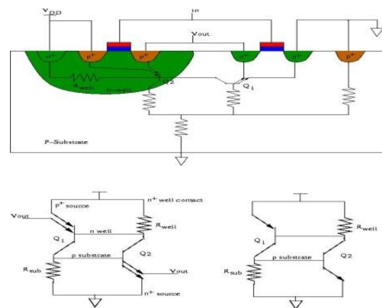
For saturation region ie $V_{DS} > (V_{GS}-V_T)$

$$I_D = \beta[V_{GS} - V_T]^2(1 - \lambda.V_{DS})$$

$$\text{Where } \beta = \frac{\mu_O.C_{OX}\left[\frac{W}{L}\right]}{2} \quad \text{Known as the transconductance parameter}$$

Full analysis 8 marks and step wise marks can be assigned.

Q 2 a) Discuss Latch-up in CMOS circuit. State its perversion.



- Latch is the generation of a low-impedance path in CMOS chips between the power supply and the ground rails due to interaction of parasitic pnp and npn bipolar transistors. These BJTs for a silicon-controlled rectifier with positive feedback and virtually short circuit the power and the ground rail.
- This causes excessive current flows and potential permanent damage to the devices.
- Analysis of the a CMOS Inverter CMOS depicting the parasitics.

Preventions:

- Reduce the BJT gains by lowering the minority carrier lifetime through Gold doping of the substrate (solution might cause excessive leakage currents).
- Use p^+ guardband rings connected to ground around nMOS transistors and n^+ guard rings connected to V_{DD} around pMOS transistors to reduce R_w and R_{sub} and to capture injected minority carriers before they reach the base of the parasitic BJT.
- Place substrate and well contacts as close as possible to the source connections of the MOS transistors to reduce the values of R_w and R_{sub}. (solution to be used in your designs)
- Place source diffusion regions for the pMOS transistors so that they lie along equi-potentials lines when currents flow between VDD and p-wells.
- Avoid forward biasing of the source/drain junctions so as not to inject high currents , this solution calls for the use of slightly doped epitaxial layer on top of the heavily doped substrate and has the effect of shunting the lateral currents from the vertical transistor through the low resistance substrate.

Latch up with Diagram 2 marks and prevention 2 marks.

Q2 b) Differentiate CMOS AND BiCMOS with respective to its electrical properties.

Any 4 properties each 1 mark.

Q2 c) Write a note on transistor gate parasitic.

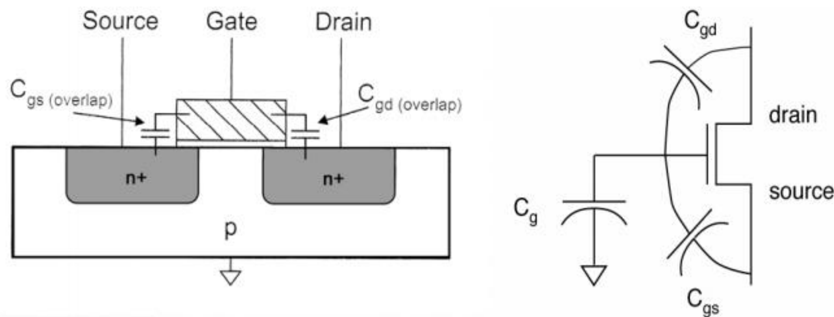
Formula for parallel plate capacitance:

$C_{ox} = \varepsilon_{ox} / x_{ox}$

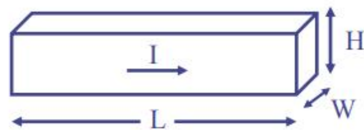
Permittivity of silicon:

$\varepsilon_{ox} = 3.46 \times 10^{-13}$ F/cm

Gate-source/drain overlap capacitance:



Q2 d) Derive a sheet resistance of wire.



$$R = \rho \times \frac{L}{A} = \frac{\rho}{H} \times \frac{L}{W} = \rho_{sq} \times \frac{L}{W}$$

$$\rho_{sq} = \text{Sheet Resistance} = \Omega/\text{sq}$$

Discuss Each parameters of above 4 steps each step 1 mark.