DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103
Mid Semester Examination – October - 2017

Branch:M.Tech (Electrical Power System) **Sem.:- I**

Subject with Subject Code:-Advanced Power Electronics(MTEPS103/MTEE102)

Marks: 20

Date:-10/10/2017 **Time:- 1 Hr.**

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Marking Scheme

(Marks)

Q.No.1 **Attempt any one of the following** **(08)**

a.) Explain the basic structure of MOSFET in detail with neat diagram.

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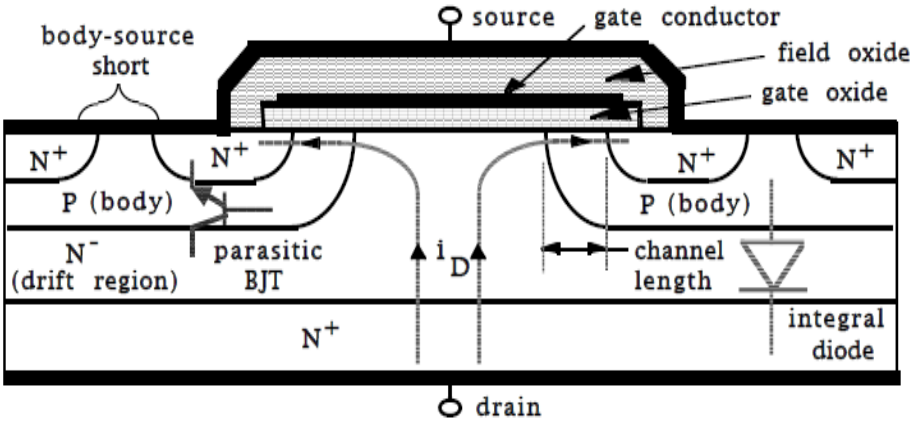
- **Explanation of the basic structure of MOSFET in detail :-04**
- **Figure of Vertical Cross Section:- 01**



1. Parasitic BJT. Held in cutoff by body-source short

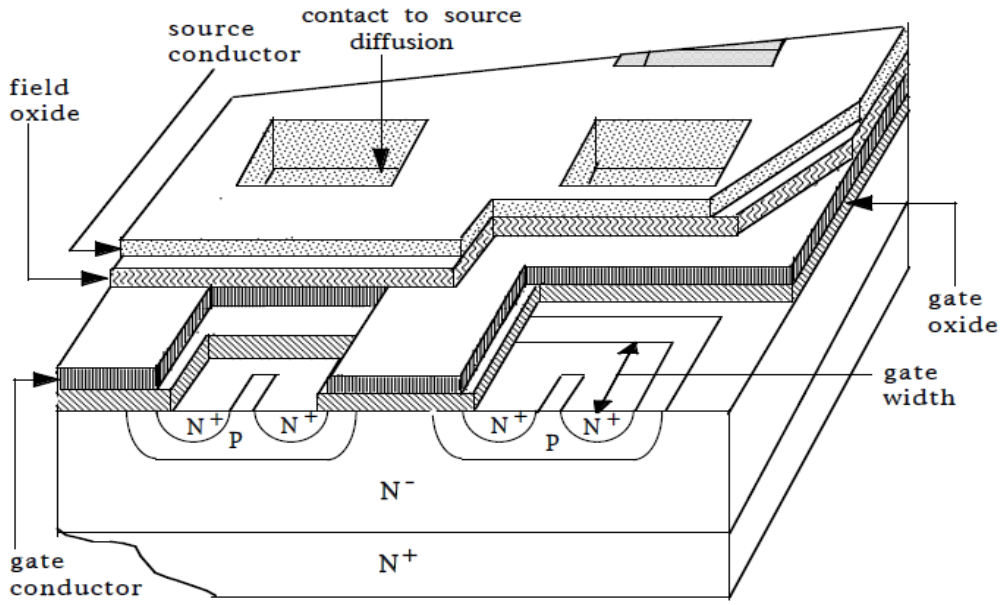
2. Integral anti-parallel diode. Formed from parasitic BJT.

3. Extension of gate metallization over drain drift region. Field plate and accumulation layer functions.

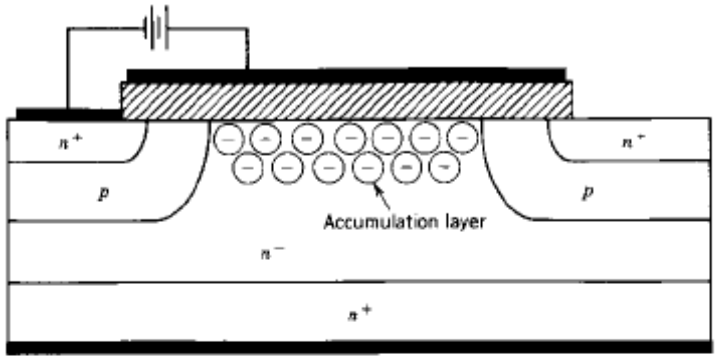
4. Division of source into many small areas connected electrically in parallel. Maximizes gate width-to-channel length ratio in order to increase gain.

5. Lightly doped drain drift region. Determines blocking voltage rating.

- **Figure of Perspective view of an n-channel or p-channel:-01**



- **Figure of gate electrode overlapping the drain drift region & Symbol of MOSFET:-02**



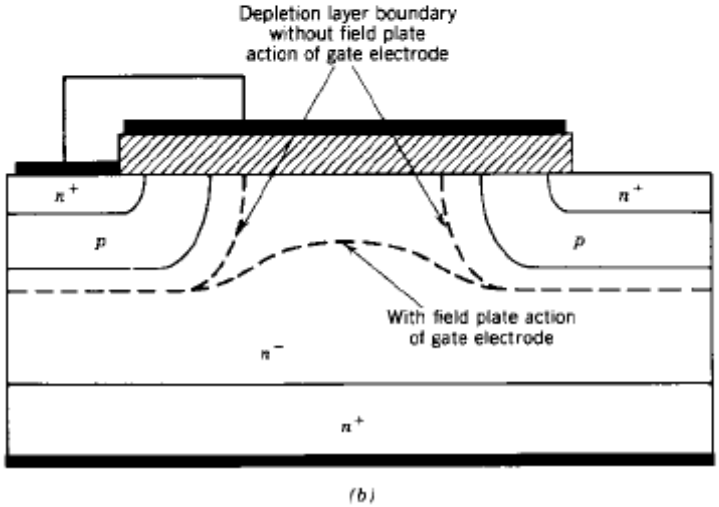


Figure of gate electrode overlapping the drain drift region (a) to create an accumulated layer in the on state, (b) to act as a field plate in off state

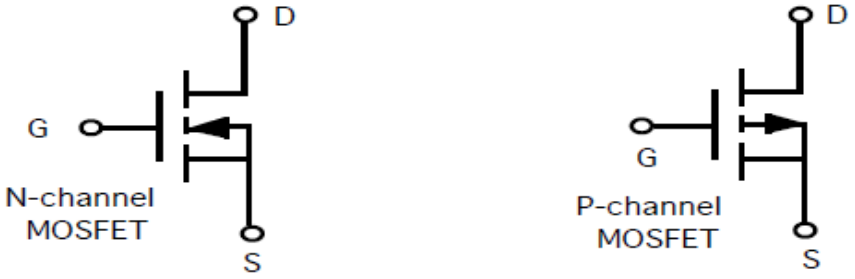


Figure of circuit symbol of MOSFET

b.) Explain the three phase semi converter with continuous output voltage.

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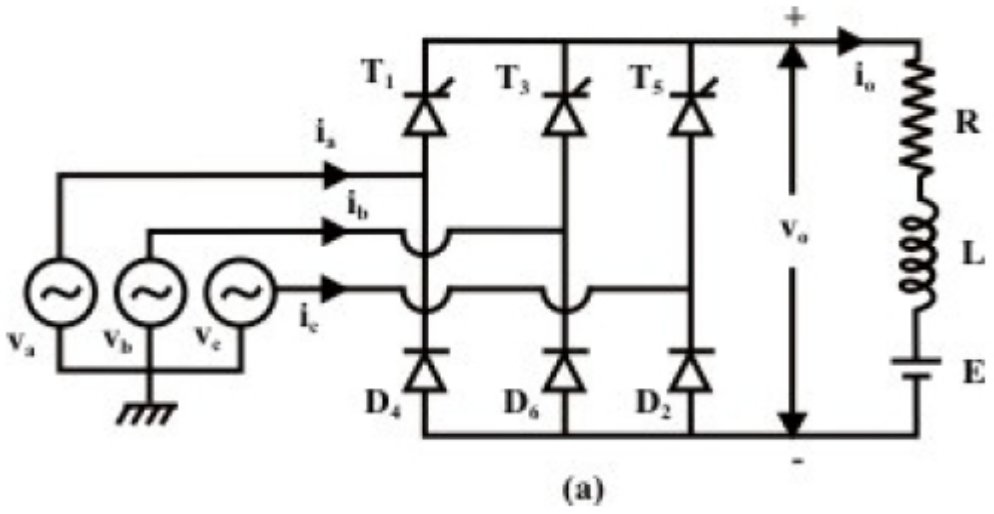
- **Explanation of three phase semi converter with circuit diagram:-04**



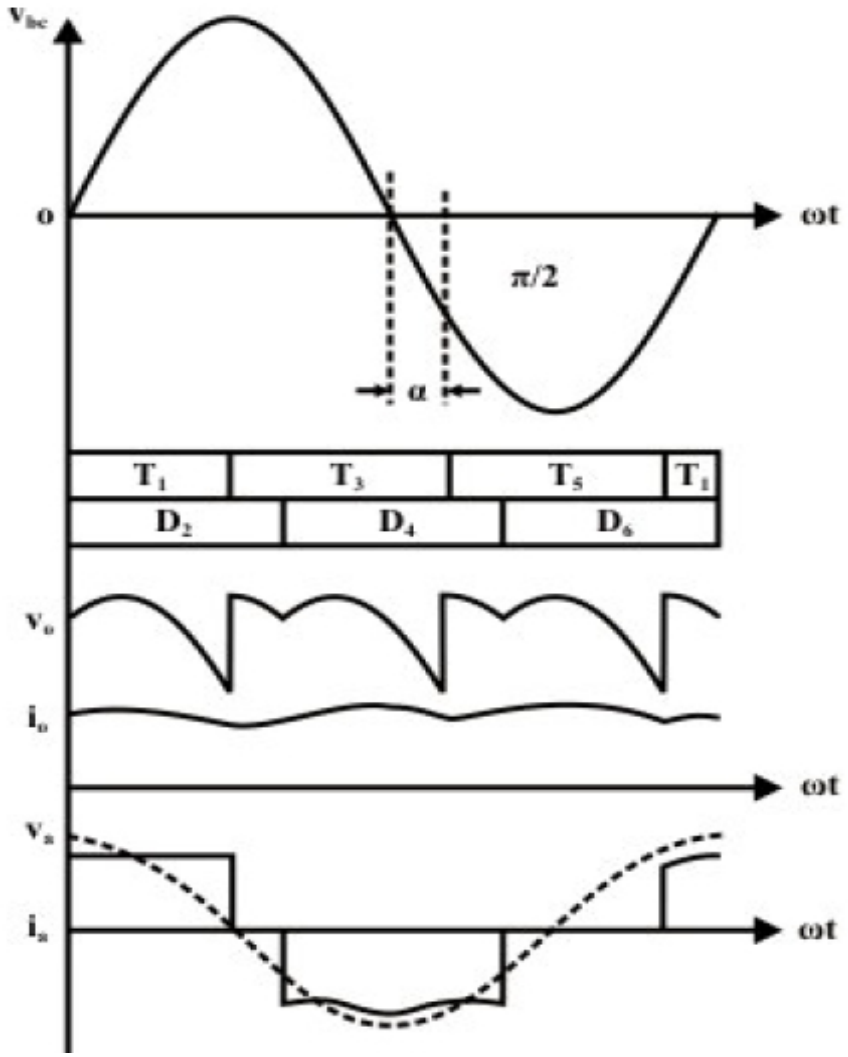
(a)

Mode / Volt	T_1D_2	D_2T_3	T_3D_4	D_4T_5	T_5D_6	D_6T_1	T_1D_4	T_3D_6	T_5D_2
V_{T1}	0	V_{ab}	V_{ab}	V_{ac}	V_{ac}	0	0	V_{ab}	V_{ac}
V_{D2}	0	0	V_{ac}	V_{ac}	V_{bc}	V_{bc}	V_{ac}	V_{bc}	0
V_{T3}	V_{ba}	0	0	V_{bc}	V_{bc}	V_{ba}	V_{ba}	0	V_{bc}
V_{D4}	V_{ca}	V_{ca}	0	0	V_{ba}	V_{ba}	0	V_{ba}	V_{ca}
V_{T5}	V_{ca}	V_{cb}	V_{cb}	0	0	V_{ca}	V_{ca}	V_{cb}	0
V_{D6}	V_{cb}	V_{cb}	V_{ab}	V_{ab}	0	0	V_{ab}	0	V_{cb}
V_0	V_{ac}	V_{bc}	V_{ba}	V_{ca}	V_{cb}	V_{ab}	0	0	0

(b)

Figure of Three phase Semi converter (a) Circuit Diagram (b) Conduction Table

- **Waveform with explanation:- 02**



Waveform of Continuous output voltage

- **Derivation of continuous output voltage and load current with boundary conditions and intervals:- 02**

Q.No. 2 Attempt any three of the following: (12)

a.) Draw the basic structure, equivalent circuit, and symbol of MCT.

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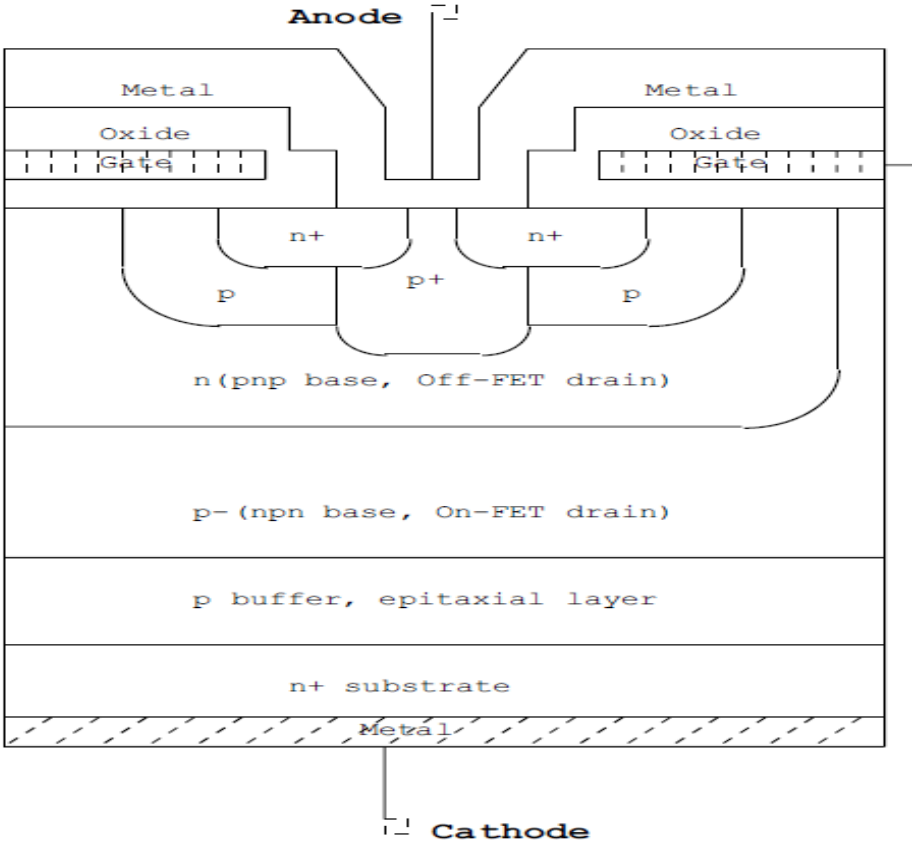
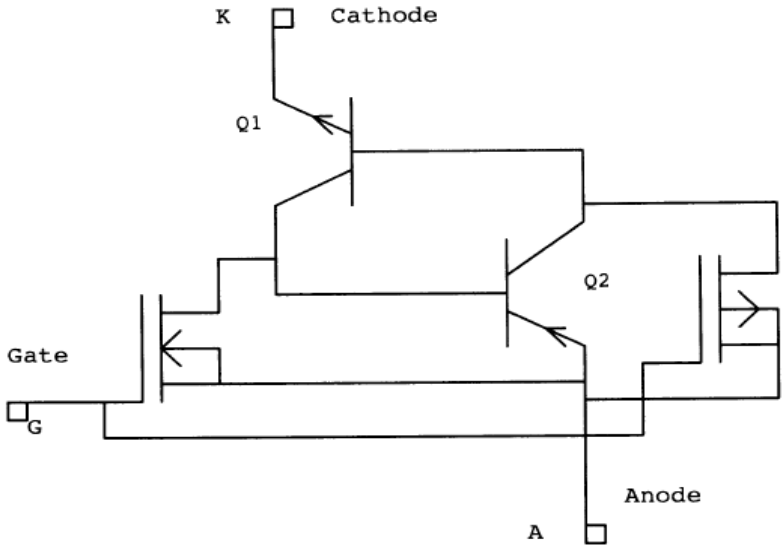
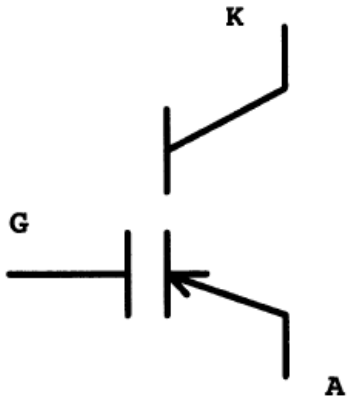
- **Figure of Basic Structure of MCT:-02**



- **Figure of equivalent circuit of MCT:-01**



- **Figure of Symbol of MCT:-01**



b.) Write short notes on snubber circuit.

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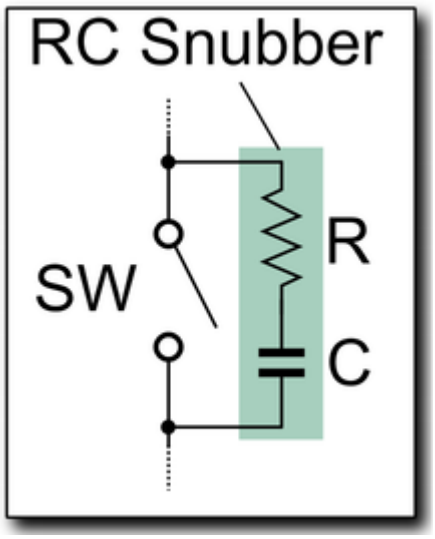
- **Types of snubber circuit:-**

1. RC snubbers



2. Diode snubbers
3. RCD snubbers
All diagram :-01
Explanation of each:-01

c.) How is the output voltage of a sinusoidal PWM Control converter varied?

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- **Waveform of Gate pulse generation with reference signal and carrier signal:-02**
- **Explanation of waveform with PF improvement:-02**

d.) Write in details methods of improving di/dt ratings of thyristor.

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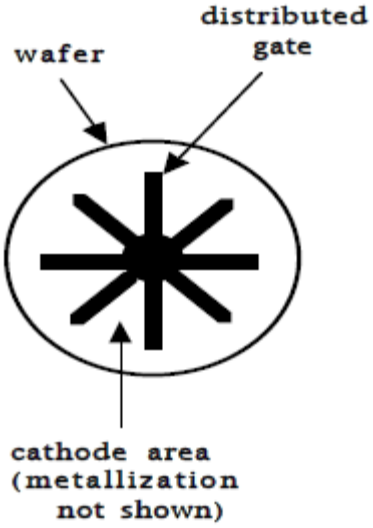
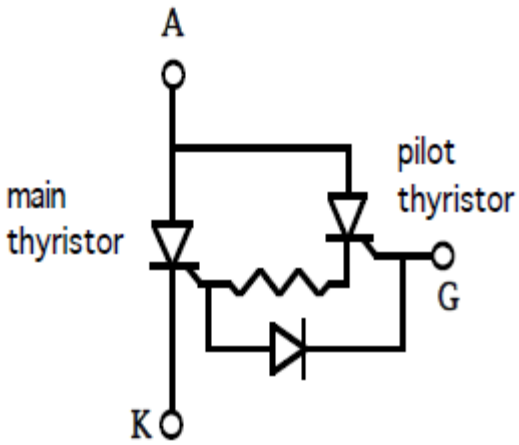
- **Figure of Thyristor with an auxiliary thyristor and gate assisted turn off thyristor:-02**





- **Explanation of following points :- 02**
- Interdigitated gate-cathode structure used to greatly increase gate-cathode periphery.
- Distance from periphery to center of any cathode region significantly shortened.
- Ability of negative gate current to break latching condition in on-state increased.
- Combination of pilot thyristor, diode, and interdigitated gate-cathode geometry termed a gate-assisted turn-off thyristor or GATT
- Use of pilot thyristor to increase turn-on gate current to main thyristor.
- Larger gate current increases amount of initial conducting area of cathode and thus improves diF/dt capabilities.
- Diode allows negative gate current to flow from main SCR.