Course Structure and Syllabus

For
M. Tech. (VLSI)
Two Year (Four Semester) Course
(w.e.f. July 2017)
M.Tech. (VLSI)

Objectives:

I. To serve the society and nation, by providing high quality engineering educational programs to the students, engaging in research and innovations that will enhance the skill and knowledge and assisting the economic development of the region, state, and nation through technology transfer.

II. To equip the postgraduate students with the state of the art education through research and collaborative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.

III. To encourage the post-graduates students, to acquire the academic excellence and skills necessary to work as Electronics and Telecommunication professional in a modern, ever-evolving world.

IV. To provide the broad understanding of social, ethical and professional issues of contemporary engineering practice and related technologies, as well as professional, ethical, and societal responsibilities.

V. To inculcate the skills for perusing inventive concept to provide solutions to industrial, social or nation problem.

Outcomes:

I. Students of this program will have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.

II. Postgraduate students will gain an ability to design and conduct experiments, as well as to analyze and interpret data/results.

III. Learners of this program will built an ability to design and develop a system, components, devices, or process to meet desired needs.

IV. Masters students of this program will have an ability to work on multi-disciplinary teams and also as an individual for solving issues related to Electronics and Telecommunication.

V. Learners of this program will have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

VI. Postgraduate students will have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.

VII. Postgraduate students will have an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.

VIII. Learners of this program will have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, and user friendliness to cater needs for innovative product development.

IX. Postgraduate students will have an ability to solve contemporary social and industrial problems by engaging in life-long learning.
### Dr. Babasaheb Ambedkar Technological University
Teaching and Examination Scheme for
M.Tech. (VLSI) w.e.f. July 2017

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Code</th>
<th>Name of the course</th>
<th>Hours/Week</th>
<th>Credit</th>
<th>Examination scheme</th>
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#### First Semester

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<tr>
<td>01</td>
<td>MTVLC101</td>
<td>Graph Theory and Discrete Optimization</td>
<td>03</td>
<td>--</td>
<td>1</td>
<td>04</td>
<td>60</td>
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<tr>
<td>02</td>
<td>MTVLC102</td>
<td>Analog IC Design</td>
<td>03</td>
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<tr>
<td>03</td>
<td>MTVLC103</td>
<td>Basics of VLSI</td>
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<td>04</td>
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<td>MTVLE114</td>
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<td>06</td>
<td>MTVLC106</td>
<td>Communication Skills</td>
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<td>07</td>
<td>MTVLL107</td>
<td>PG Lab-I*</td>
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**Total for Semester I**: 17 L 03 P 03 T 22 300 100 150 50 600

#### Second Semester

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<tbody>
<tr>
<td>01</td>
<td>MTVLC201</td>
<td>VLSI System Testing</td>
<td>03</td>
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<td>02</td>
<td>MTVLC202</td>
<td>Design of ASICs</td>
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<td>07</td>
<td>MTVLP207</td>
<td>Mini-Project</td>
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**Total for Semester II**: 15 L 8 P 02 T 21 300 100 200 100 700

#### Third Semester

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<td>1</td>
<td>MTVLC301</td>
<td>Project Management &amp;Intellectual Property</td>
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**Total for Semester III**: -- L -- P -- T 12 -- -- 100 100 200

#### Fourth Semester

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<td>100 100 200</td>
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</table>

**Total for Semester IV**: -- L -- P -- T 20 -- -- 100 100 200

**GRAND TOTAL**: 1700

* PG Lab-I –Practical shall be based on courses of first semester.

# Student has to choose this course either from NPTEL/MOOC pool and submission of course completion certificate is mandatory.
Elective-I

A. Digital System Design
B. Modeling and Synthesis with Verilog HDL
C. Optimization of Digital Signal Processing structures for VLSI
D. Cognitive Radio
E. VLSI Process Technology

Elective-II

A. Advanced Computer Architecture
B. Low Power VLSI circuits
C. VLSI Digital Signal Processing Systems
D. Advanced Digital Design
E. RF circuits
F. Mixed - Signal Circuit Design

Elective-III

A. Functional Verification using Hardware Verification Languages
B. High Speed System Design
C. High Speed Communication Networks
D. DSP Architecture
E. RF MEMS

Elective-IV

A. Computer Aided Design for VLSI
B. Semiconductor Memory Design and Testing
C. FPGA System Design
D. Nanoscale Devices and Circuit Design
E. Analysis and Design of Digital Systems using VHDL

Elective-V (Open)

A. ASIC & SOC
B. IC Technology
C. Linear Algebra
D. Research Methodology
E. Internet of Things
**Course Objective:**

A  
To introduce the basics of graphs and combinatory required for VLSI design and Optimization.

**Course Outcomes:**

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand the various types of graph Algorithms and graph theory properties.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to analyze the NP – complete problems.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to distinguish the features of the various tree and matching algorithms</td>
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<tr>
<td>CO4</td>
<td>Learner will be able to understand applications of digraphs and graph flow.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the linear programming principles and its conversion.</td>
</tr>
</tbody>
</table>

**UNIT I**

Basic definitions, Degree of vertices, Complement of a graph. Self-complementary graph, some eccentricity properties of graphs. Tree, spanning tree. Directed graphs standard definitions; strongly, weakly, unilaterally connected digraphs, deadlock communication network. Matrix representation of graph and digraphs.

**UNIT II**

Eulerian graphs and standard results relating to characterization. Hamiltonian graph-standard theorems (Dirac theorem, Chavathal theorem, closure of graph). Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.

**UNIT III**

Chromatic number; Vertex and edge (only properties and examples)-application to colouring. Planar graphs, Euler’s formula, maximum number of edges in a planar graph. Five colour theorem. DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, planarity algorithm. Matching theory, maximal matching and algorithms form aximal matching. Perfect matching (only properties and applications to regular graphs).

**UNIT IV**

Flows in graphs, Ranking of participants in tournaments, simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.
UNIT V
Linear- Integer Linear programming, Conversion of TSP, maxflow, Knapsack scheduling, shortest path problems for Linear programming types - branch bound method to solve

UNIT VI
Knapsack problems- critical path and linear programming conversion- Floor shop scheduling problem- Personal assignment problem.
Dynamic programming- TSP- compartment problems- Best investment problems.

TEXTBOOKS /REFERENCE:
4. Recent literature in Graph Theory and Discrete Optimization.
ANALOG IC DESIGN

Weekly Teaching Hours TH : 03    Tut:    01
Scheme of Marking TH :60    Tests : 20    IA: 20    Total : 100

Course Objective:

A To develop the ability design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.

B To develop the skills to design analog VLSI circuits for a given specification.

Course Outcomes:

| CO1 | Learner will be able to understand equivalent circuits of MOS based Analog VLSI and analyze their performance.
| CO2 | Learner will be able to design analog VLSI circuits for a given specification.
| CO3 | Learner will be able to analyze the frequency response of the different configurations of an amplifier.
| CO4 | Learner will be able to understand the feedback topologies involved in the amplifier design.
| CO5 | Learner will be able to design features of the differential amplifiers.

UNIT I
Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT II

UNIT III

UNIT IV
Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading.
UNIT V

UNIT VI
Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.

TEXTBOOKS / REFERENCE::
6. Recent literature in Analog IC Design.
BASICS OF VLSI

Weekly Teaching Hours
TH : 03  Tut: 01

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objective:

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<tbody>
<tr>
<td>A</td>
<td>To provide rigorous foundation in MOS and CMOS digital circuits.</td>
</tr>
<tr>
<td>B</td>
<td>To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity</td>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to implement the logic circuits using MOS and CMOS technology.</td>
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<tr>
<td>CO2</td>
<td>Learner will be able to analyze various circuit configurations and their applications.</td>
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<tr>
<td>CO3</td>
<td>Learner will be able to analyze the merits of circuits according to the technology and applications change.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to design low power CMOS VLSI circuits.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the rapid advances in CMOS Technology.</td>
</tr>
</tbody>
</table>

UNIT I
Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow.

UNIT II
MOS transistor theory: Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

UNIT III
CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues.

UNIT IV
Circuit characterization and performance estimation: Delay estimation, Logical effort and Transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

UNIT V

UNIT VI
Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.
TEXTBOOKS / REFERENCE::
4. Recent literature in Basics of VLSI.
ELECTIVE-I
DIGITAL SYSTEM DESIGN

Weekly Teaching Hours TH : 03 Tut: --
Scheme of Marking TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:

A To get an idea about designing complex, high speed digital systems and how to implement such design

Course Outcomes:

| CO1 | Learner will be able to identify mapping algorithms into architectures. |
| CO2 | Learner will be able to understand various delays in combinational circuit and its optimization methods. |
| CO3 | Learner will be able to understand circuit design of latches and flip-flops |
| CO4 | Learner will be able to demonstrate combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices. |
| CO5 | Learner will be able to understand the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable. |

UNIT I
Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

UNIT II

UNIT III

UNIT IV
Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division.

UNIT V
SRAM, DRAM, ROM, serial access memory, context addressable memory.

UNIT VI
Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures-Single context, Multi context, partially reconfigurable, Pipeline reconfigurable,
Block Configurable, Parallel processing.

TEXTBOOKS / REFERENCE:

9. Recent literature in Digital System Design.
ELECTIVE-I
MODELING AND SYNTHESIS WITH VERILOG HDL

Weekly Teaching Hours   TH : 03    Tut:  --
Scheme of Marking       TH :60    Tests : 20    IA: 20    Total : 100

Course Objective:

A  To design combinational, sequential circuits using Verilog HDL.
B  To understand behavioral and RTL modeling of digital circuits.
C  To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools.
D  To simulate, synthesize, and program their designs on a development board.
E  To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand the basic concepts of verilog HDL</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to demonstrate digital systems in verilog HDL at different levels of abstraction</td>
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<tr>
<td>CO3</td>
<td>Learner will be able to understand the simulation techniques and test bench creation.</td>
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<tr>
<td>CO4</td>
<td>Learner will be able to understand the design flow from simulation to synthesizable version</td>
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<tr>
<td>CO5</td>
<td>Learner will be able to understand the process of synthesis and post-synthesis</td>
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</tbody>
</table>

UNIT I
Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

UNIT II
Logic system, data types and operators for modeling inverilog HDL.

UNIT III
Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.

UNIT IV
Behavioral descriptions in verilogHDL. Synthesis of combinational logic.
UNIT V
HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

UNIT VI
Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

TEXTBOOKS / REFERENCE:

5. Recent literature in Modeling and Synthesis with Verilog HDL.
ELECTIVE-I

OPTIMIZATIONS OF DIGITAL SIGNAL PROCESSING STRUCTURES FOR VLSI

Weekly Teaching Hours TH : 03 Tut: --
Scheme of Marking TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:

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<tbody>
<tr>
<td>A</td>
<td>To understand the various VLSI architectures for digital signal processing.</td>
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<td>B</td>
<td>To know the techniques of critical path and algorithmic strength reduction in the filter structures.</td>
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<tr>
<td>C</td>
<td>To enable students to design VLSI system with high speed and low power.</td>
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<tr>
<td>D</td>
<td>To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.</td>
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</table>

Course Outcomes:

| CO1 | Learner will be able to understand the overview of DSP concepts and design architectures for DSP algorithms. |
| CO2 | Learner will be able to improve the overall performance of DSP system through various transformation and optimization techniques. |
| CO3 | Learner will be able to perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power. |
| CO4 | Learner will be able to optimize design in terms of computation complexity and speed. |
| CO5 | Learner will be able to understand clock based issues and design asynchronous and wave pipelined systems. |

UNIT I

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

UNIT II

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding

UNIT III

UNIT IV
Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

UNIT V
Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs.

UNIT VI
Wave pipelining, constraint space diagram and degree of wavepipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

TEXTBOOKS / REFERENCE:

ELECTIVE-I
COGNITIVE RADIO

Weekly Teaching Hours
TH : 03    Tut: --

Scheme of Marking
TH : 60    Tests : 20    IA : 20    Total : 100

Course Objectives:

A  To understand the use of the SDR
B  To understand the stages of the evolution of SDR.
C  To study the applications of the Cognitive Radio.
D  To develop the system model for the spectrum sensing and spectrum access techniques in CR.

Course Outcomes:

CO1  Learner will be able to differentiate between SDR and CR
CO2  Learner will be able to evaluate the different spectrum sensing techniques for the cognitive radio.
CO3  Learner will be able to develop the system model for single carrier and multicarrier cognitive radio system.
CO4  Learner will be able to evaluate the different spectrum management techniques for cognitive radio system.
CO5  Learner will be able to simulate and analyze the SDR and Cognitive radio systems

UNIT I

UNIT II
Cooperative Communications and Networks - Information Theory for Cooperative Communications, Fundamental Network Information, Multiple-access Channel with Cooperative Diversity, Cooperative Communications, Three-Node Cooperative Communications, Multiple-Node Relay Network, Cooperative Wireless Networks, Benefits of Cooperation in Wireless Networks, Cooperation in Cluster-Based Ad-hoc Networks

UNIT III

UNIT IV


UNIT V


UNIT VI


Text/Reference Books:

3. Qusay H. Mahmoud, Cognitive Networks, John Wiley & Sons Ltd.
ELECTIVE-I
VLSI PROCESS TECHNOLOGY

Weekly Teaching Hours
TH : 03
Tut: --

Scheme of Marking
TH : 60
Tests : 20
IA: 20
Total : 100

Course Objective:
A
To provide rigorous foundation in MOS and CMOS fabrication process.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand various techniques involved in the VLSI fabrication process.</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to understand the different lithography methods and etching process</td>
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<tr>
<td>CO3</td>
<td>Learner will be able to analyze the deposition and diffusion mechanisms.</td>
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<tr>
<td>CO4</td>
<td>Learner will be able to analyze the fabrication of NMOS, CMOS memory and bipolar devices</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the nuances of assembly and packaging of VLSI devices.</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II
Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

UNIT III

UNIT IV
Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition.

UNIT V
NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

UNIT VI
Analytical and assembly techniques. Packaging of VLSI devices.
TEXTBOOKS / REFERENCE:

ELECTIVE-II
ADVANCED COMPUTER ARCHITECTURE

Weekly Teaching Hours
TH : 03 Tut: --

Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:

| A | To give an exposure on look ahead pipelining- parallelism, multiprocessor scheduling, multithreading and various memory organizations. |

Course Outcomes:

| CO1 | Learner will be able to apply the basic knowledge of partitioning and scheduling in Multiprocessors. |
| CO2 | Learner will be able to analyze and design cache memory, virtual memory and shared memory organizations. |
| CO3 | Learner will be able to distinguish and analyze the design properties of Linear and Non – Linear processors. |
| CO4 | Learner will be able to analyze the principles of multithreading in hybrid Architectures. |
| CO5 | Learner will be able to analyze any parallel programming models for various architectures and Applications. |

UNIT I

UNIT II

UNIT III

UNIT IV
UNIT V
Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes.

UNIT VI
Message passing program development. Mapping programs onto multicomputer. Multiprocessor UNIX design goals. MACH/OS kernel architecture. OSF/1 architecture and applications.

TEXTBOOKS / REFERENCE:

4. Recent literature in Advanced Computer Architecture.
ELECTIVE-II
LOW POWER VLSI CIRCUITS

Weekly Teaching Hours
TH : 03    Tut:   --

Scheme of Marking
TH :60    Tests : 20  IA: 20    Total : 100

Course Objective:

A  To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit design.

Course Outcomes:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to acquire the knowledge about various CMOS fabrication process and its modeling.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to infer about the second order effects of MOS transistor characteristics.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze and implement various CMOS static logic circuits.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand the design of various CMOS dynamic logic circuits.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the design techniques low voltage and low power CMOS circuits for various applications.</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to understand the different types of memory circuits and their design.</td>
</tr>
<tr>
<td>CO7</td>
<td>Learner will be able to design and implement various structures for low power applications.</td>
</tr>
</tbody>
</table>

UNIT I
Evolution of CMOS technology. 0.25 µm and 0.1 µm technologies. Shallow trench isolation. Lightly-doped drain. Buried channel. BiCMOS and SOI CMOS technologies. Second order effects and capacitance of MOS devices.

UNIT II
CMOS inverters, static logic circuits of CMOS, pass transistors, BiCMOS, SOI CMOS and low power CMOS techniques

UNIT III
Basic concepts of dynamic logic circuits. Various problems associated with dynamic logic circuits.

UNIT IV
Differential, BiCMOS and low voltage dynamic logic circuits.

UNIT V
Different types of memory circuits
UNIT VI
Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

TEXTBOOKS / REFERENCE:

4 Recent literature in Low Power VLSI Circuits.
ELECTIVE-II
VLSI DIGITAL SIGNAL PROCESSING SYSTEMS

Weekly Teaching Hours
TH : 03 Tut: --

Course Objective:
<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>To enable students to design VLSI systems with high speed and low power.</td>
</tr>
<tr>
<td>B</td>
<td>To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.</td>
</tr>
</tbody>
</table>

Course Outcomes:
| CO1 | Learner will be able to acquire the knowledge of round off noise computation and numerical strength reduction. |
| CO2 | Learner will be able to design Bit level and redundant arithmetic Architectures. |

UNIT I

UNIT II

UNIT III
Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

UNIT IV
Redundant arithmetic -Redundant number representations, carry free radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures, data format conversion, Redundant to Non-redundant converter.

UNIT V
Numerical Strength Reduction - Sub expression Elimination, Multiple Constant Multiplication,

UNIT VI
Sub expression sharing in Digital Filters, Additive and Multiplicative Number Splitting.
TEXTBOOKS / REFERENCE:

3 Recent literature in VLSI Digital Signal Processing Systems.
ELECTIVE-II
ADVANCED DIGITAL DESIGN

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objective:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>To make the students learn about graphical models and state diagram in designing optimized digital circuits.</td>
</tr>
<tr>
<td>B</td>
<td>To provide the students a detailed knowledge of scheduling algorithm, synthesis of pipelined circuits and scheduling pipelined circuits</td>
</tr>
<tr>
<td>C</td>
<td>To enable the students to design digital design with advanced technique like Sequential logic optimization and test the designed circuit Testability considerations.</td>
</tr>
</tbody>
</table>

Course Outcomes:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand advanced state of art techniques of digital design.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to synthesize the circuits and evaluate its performance in terms of area, power and speed.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand use of scheduling algorithm.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to gain in-depth knowledge of sequential digital circuits designed using resource sharing.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand synchronization across clock domains, timing analysis, and Testability considerations</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II

UNIT III
Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.

UNIT IV
UNIT V
Sequential logic optimization-sequential circuit optimization using state based models and network models

UNIT VI
Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits.

TEXTBOOKS / REFERENCE:

8. Recent literature in Advanced Digital Design.
ELECTIVE-II
RF CIRCUITS

Weekly Teaching Hours
TH: 03  Tut: --

Scheme of Marking
TH: 60  Tests: 20  IA: 20  Total: 100

Course Objective:
A  To impart knowledge on basics of IC design at RF frequencies.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand the Noise models for passive components and noise theory</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to analyze the design of a high frequency amplifier</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand the different LNA topologies &amp; design techniques</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to distinguish between different types of mixers</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to analyze the various types of synthesizers, oscillators and their characteristics.</td>
</tr>
</tbody>
</table>

UNIT I
Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, noise models for active and passive components

UNIT II
High frequency amplifier design – zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization

UNIT III
Low noise amplifier design – LNA topologies, power constrained noise optimization, linearity and large signal performance

UNIT IV
Mixers – multiplier-based mixers, subsampling mixers, diode-ring mixers RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.

UNIT V
Oscillators: describing functions, resonators, negative resistance oscillators,

UNIT VI
Synthesizers: synthesis with static moduli, synthesis with dithering moduli, combination synthesizers - phase noise considerations.
TEXTBOOKS / REFERENCE:

6. Recent literature in RF Circuits.
ELECTIVE-II
MIXED - SIGNAL CIRCUIT DESIGN

Weekly Teaching Hours  TH: 03  Tut:  --
Scheme of Marking    TH:60  Tests: 20  IA: 20  Total: 100

Course Objective:

A  To make the students to understand the design and performance measures concept of mixed signal circuit.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO</th>
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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand the fundamentals of data converters and also optimized their performances.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to understand the design methodology for mixed signal IC design using gm/Id concept.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze the design of current mirrors and operational amplifiers</td>
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<tr>
<td>CO4</td>
<td>Learner will be able to design the CMOS digital circuits and implement its layout.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to design the frequency and Q tunable time domain filters.</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II
Fundamentals of DataConverters.Nyquist Rate Converters and Over sampling Converters.

UNIT III
Design methodology for mixed signal IC design using gm/Id concept.

UNIT IV

UNIT V
CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

UNIT VI
Design of frequency and Q tunable continuous time filters.

TEXTBOOKS / REFERENCE:
COMMUNICATION SKILLS

Weekly Teaching Hours
TH: 02
Practical: -

Scheme of Marking
TH: --
IA: 25
PR/OR: 25
Total: 50

Course Objectives:

| A | To become more effective confident speakers and deliver persuasive presentations |
| B | To develop greater awareness and sensitivity to some important considerations in interpersonal communication and learn techniques to ensure smoother interpersonal relations |

Course Outcomes:

| CO1 | Learner will be able to understand the fundamental principles of effective business communication |
| CO2 | Learner will be able to apply the critical and creative thinking abilities necessary for effective communication in today's business world |
| CO3 | Learner will be able to organize and express ideas in writing and speaking to produce messages suitably tailored for the topic, objective, audience, communication medium and context |
| CO4 | Learner will be able to demonstrate clarity, precision, conciseness and coherence in your use of language |
| CO5 | Learner will be able to become more effective confident speakers and deliver persuasive presentations |

UNIT I
Introduction to communication, Necessity of communication skills, Features of good communication, Speaking skills, Feedback & questioning technique, Objectivity in argument

UNIT II
Verbal and Non-verbal Communication, Use and importance of non-verbal communication while using a language, Study of different pictorial expressions of non-verbal communication and their analysis

UNIT III
Academic writing, Different types of academic writing, Writing Assignments and Research Papers, Writing dissertations and project reports

UNIT IV
Presentation Skills: Designing an effective Presentation, Contents, appearance, themes in a presentation; Tone and Language in a presentation, Role and Importance of different tools for effective presentation

UNIT V
Motivation/ Inspiration: Ability to shape and direct working methods according to self-defined criteria; Ability to think for oneself, Apply oneself to a task independently with self-motivation, Motivation techniques: Motivation techniques based on needs and field situations
UNIT VI
Self-management, Self-evaluation, Self-discipline, Self-criticism, Recognition of one’s own limits and deficiencies, dependency etc. Self-awareness, Identifying one’s strengths and weaknesses, Planning & Goal setting, Managing self-emotions, ego, pride leadership & Team dynamics

TEXTBOOKS / REFERENCE:

PG LAB-I

Weekly Teaching Hours  TH: --  Practical: 03

Scheme of Marking  TH: --  IA: 25  PR/OR: 25  Total: 50

Practical’s of the Lab - I shall be based on the courses of first semester. The lab work shall consist of hands on experiments on the different software and hardware platforms related to the syllabus.
VLSI SYSTEM TESTING

Weekly Teaching Hours
TH : 03  Tut:  01

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objective:

| A | To expose the students, the basics of testing techniques for VLSI circuits and Test Economics. |

Course Outcomes:

| CO1 | Learner will be able to apply the concepts in testing which can help them design a better yield in IC design. |
| CO2 | Learner will be able to tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs. |
| CO3 | Learner will be able to analyze the various test generation methods for static & dynamic CMOS circuits. |
| CO4 | Learner will be able to identify the design for testability methods for combinational & sequential CMOS circuits. |
| CO5 | Learner will be able to recognize the BIST techniques for improving testability. |

UNIT I

UNIT II
Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

UNIT III

UNIT IV
Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

UNIT V
Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve Testability.
UNIT VI
Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

TEXTBOOKS / REFERENCE:

6. Recent literature in VLSI System Testing.
DESIGN OF ASICS

Weekly Teaching Hours
TH : 03   Tut:  01

Scheme of Marking
TH :60   Tests : 20   IA: 20   Total : 100

Course Objective:

A  To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
B  To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
C  To give the student an understanding of basics of System on Chip and Platform based design.
D  To give the student an understanding of High performance algorithms

Course Outcomes:

CO1 Learner will be able to demonstrate VLSI tool-flow and appreciate FPGA and CPLD architectures
CO2 Learner will be able to understand the issues involved in ASIC design, including technology choice, design management and tool-flow.
CO3 Learner will be able to understand the algorithms used for ASIC construction
CO4 Learner will be able to understand Full Custom Design Flow and Tool used
CO5 Learner will be able to understand Semicustom Design Flow and Tool used - from RTL to GDS and Logical to Physical Implementation
CO6 Learner will be able to understand about STA, LEC, DRC, LVS, DFM
CO7 Learner will be able to understand the basics of System on Chip and on chip communication architectures appreciate high performance algorithms for ASICs

UNIT I
Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors.

UNIT II
UNIT III
Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.

UNIT IV

UNIT V

UNIT VI
High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

TEXTBOOKS / REFERENCE:
ELECTIVE-III
FUNCTIONAL VERIFICATION USING HARDWARE VERIFICATION LANGUAGES

Weekly Teaching Hours
TH : 03 Tut: --

Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:
A Learn to use verification tools and experiment on actual circuits designed in industry

Course Outcomes:

<table>
<thead>
<tr>
<th>CO</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>CO1</td>
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<tr>
<td>CO2</td>
<td>Learner will be able to understand the design methodology for mixed signal IC design using gm/Id concept</td>
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<td>CO3</td>
<td>Learner will be able to analyze the design of current mirrors and operational amplifiers</td>
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<tr>
<td>CO4</td>
<td>Learner will be able to design the CMOS digital circuits and implement its layout.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to design the frequency and Q tunable time domain filters.</td>
</tr>
</tbody>
</table>

UNIT I
System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Advanced OOPs & Test bench guidelines, Advanced Interfaces

UNIT II

UNIT III
System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single & Multiple Clock definitions, Implication operators (Overlapping & Non-overlapping), Repetition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match,t throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property

UNIT IV
SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology

UNIT V
Assertions: Practice & Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

UNIT VI

TEXTBOOKS / REFERENCE:

9. Recent literature in Functional Verification using Hardware Verification Languages.
ELECTIVE-III
HIGH SPEED SYSTEM DESIGN

Weekly Teaching Hours
TH : 03 Tut: -

Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:

<p>| | |</p>
<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The requirement that systems perform complex tasks in a time frame considered comfortable by humans</td>
</tr>
<tr>
<td>B</td>
<td>The ability of component manufacturers to produce high-speed devices.</td>
</tr>
</tbody>
</table>

Course Outcomes:

| CO1 | Learner will be able to understand Integrity and stability of ground and power |
| CO2 | Learner will be able to understand Termination and careful layout |
| CO3 | Learner will be able to understand Noise suppression |

UNIT I
Functions of an Electronic Package, Packaging Hierarchy, IC packaging requirements and properties; materials and substrates; Interconnect Capacitance, Resistance and Inductance fundamentals; IC assembly: Wire bonding, Tape Automated Bonding, Flip Chip, waferlevel packaging; impact on reliability and testability.

UNIT II
Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise.

UNIT III
Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers.

UNIT IV

UNIT V
Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced.
UNIT VI
Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

TEXTBOOKS / REFERENCE:

5. R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011. 5. Recent literature in High Speed System Design.
ELECTIVE-III
HIGH SPEED COMMUNICATION NETWORKS

Weekly Teaching Hours TH : 03 Tut: -
Scheme of Marking TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:
A To impart the students a thorough exposure to the various high speed networking technologies and to analyse the methods adopted for performance modeling, traffic management and routing

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to compare and analyze the fundamental principles of various high speed communication networks and their protocol architectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to analyze the methods adopted for performance modeling of traffic flow and estimation</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand the congestion control issues and traffic management in TCP/IP and ATM networks</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to compare, analyse and implement the various routing protocols in simulation software tools</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to examine the various services</td>
</tr>
</tbody>
</table>

UNIT I
The need for a protocol architecture, The TCP/IP protocol architecture, Internetworking, Packet switching networks, Frame relay networks, Asynchronous Transfer mode (ATM) protocol architecture, High speed LANs. Multistage networks

UNIT II
Overview of probability and stochastic process, Queuing analysis, single server and multiserver queues, queues with priorities, networks of queues, Self similar Data traffic.

UNIT III
Congestion control in data networks and internets, Link level flow and error control, TCP traffic control, Traffic and congestion control in ATM networks.

UNIT IV
Overview of Graph theory and least cost paths, Interior routing protocols, Exterior routing protocols and multicast.

UNIT V
Quality of service in IP networks, Integrated and differentiated services, Protocols for QOS support-Resource reservation protocol,
UNIT VI
Multiprotocol label switching, Real time transport protocol

TEXTBOOKS / REFERENCE:

5. Giroux, N. and Ganti, S.” Quality of service in ATM networks”, Prentice Hall,1999
6. Recent literature in High Speed Communication Networks.
ELECTIVE-III
DSP ARCHITECTURE
Weekly Teaching Hours
TH : 03 Tut: -
Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:
A To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors

Course Outcomes:

| CO1 | Learner will be able to understand the architecture details fixed and floating point DSPs |
| CO2 | Learner will be able to infer about the control instructions, interrupts, and pipeline operations, memory and buses. |
| CO3 | Learner will be able to understand the features of on-chip peripheral devices and its interfacing with real time application devices |
| CO4 | Learner will be able to implement the signal processing algorithms and applications in DSPs |
| CO5 | Learner will be able to understand the architecture of advanced DSPs |

UNIT I
Fixed-point DSP architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison

UNIT II

UNIT III
On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF.

UNIT IV

UNIT V
UNIT VI
Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP, CORTEX, SHARC, SIMD, MIMD Architectures.

TEXTBOOKS / REFERENCE:

6. Recent literature in DSP Architecture
ELECTIVE-III
RF MEMS

Weekly Teaching Hours	TH: 03 Tut: -
Scheme of Marking 
TH: 60 Tests: 20 IA: 20 Total: 100

Course Objective:
A To impart knowledge on basics of MEMS and their applications in RF circuit design

Course Outcomes:

<table>
<thead>
<tr>
<th>CO</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand the Micromachining Processes</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to understand the design and applications of RF MEMS inductors and capacitors</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze RF MEMS Filters and RF MEMS Phase Shifters</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand suitability of micro-machined transmission lines for RF MEMS</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the Micro-machined Antennas and Reconfigurable Antennas</td>
</tr>
</tbody>
</table>

UNIT I
Micromachining Processes - methods, RF MEMS relays and switches. Switch parameters. Actuation mechanisms. Bistable relays and micro actuators. Dynamics of switching operation

UNIT II

UNIT III
MEMS phase shifters. Types. Limitations. Switched delay lines. Fundamentals of RF MEMS Filters

UNIT IV
Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.

UNIT V
Micro-machined antennas. Microstrip antennas – design parameters.

UNIT VI
Micromachining to improve performance. Reconfigurable antennas.
TEXTBOOKS / REFERENCE:
4. Recent literature in RF MEMS.
**Elective IV**

**Computer Aided Design for VLSI**

Weekly Teaching Hours  
TH : 03  
Tut: --

Scheme of Marking  
TH :60  
Tests : 20  
IA: 20  
Total : 100

**Course Objective:**

| A | To impart knowledge on basics of MEMS and their applications in RF circuit design |

**Course Outcomes:**

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand the fundamentals of VLSI CAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to understand the simulation and design of RTL</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to demonstrate various verification methodologies</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to analyze different fundamentals of Layout Synthesis</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to design a system based on C and Verilog</td>
</tr>
</tbody>
</table>

**UNIT I**

Introduction to VLSI CAD: Motivating factors and some trends; digital hardware modeling: logic and system level modeling, hardware description languages (VHDL and Verilog)

**UNIT II**

RTL simulation; synchronous and asynchronous system design;

**UNIT III**

Verification methodology: simulation, BDD, formal methods; logic synthesis: technology mapping, ASIC design methodology, FPGA based system design and prototyping;

**UNIT IV**

Layout synthesis: the physical design, timing analysis; graph algorithms and their application in IC design;

**UNIT V**

CAD tools and their use; Design for testability

**UNIT VI**

System level design: brief mention of System C and System Verilog

**TEXT/REFERENCE BOOKS**

4. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic Publisher
ELECTIVE IV
SEMICONDUCTOR MEMORY DESIGN AND TESTING

Weekly Teaching Hours

<table>
<thead>
<tr>
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<th>TH</th>
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<tr>
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</table>

Scheme of Marking

<table>
<thead>
<tr>
<th></th>
<th>TH</th>
<th>Tests</th>
<th>IA</th>
<th>Total</th>
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<tbody>
<tr>
<td></td>
<td>60</td>
<td>20</td>
<td>20</td>
<td>100</td>
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</table>

Course Objective:

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<tbody>
<tr>
<td>A</td>
<td>Describing the structure and operation of the main types of semiconductor memory.</td>
</tr>
<tr>
<td>B</td>
<td>The different contexts in which memories are tested together with the corresponding different types of tests.</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th>CO</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand memory cell structures and fabrication technologies.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to demonstrate application–specific memories and architectures.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze memory design, fault modeling and test algorithms, limitations, and trade–offs</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to analyze general reliability issues of memory.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to analyze various effects of radiation on memory</td>
</tr>
</tbody>
</table>

UNIT I
Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT II
Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT III
Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT IV
**Semiconductor Memory Reliability:** General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification,

**UNIT V**

**Radiation Effects:**
Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

**UNIT VI**

**Advanced Memory Technologies and High-density Memory Packing Technologies:** Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

**TEXT/REFERENCE BOOKS**

ELECTIVE IV
FPGA SYSTEM DESIGN

Weekly Teaching Hours
TH : 03 Tut: --

Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objective:

A To introduce students to advanced design methodologies and practical design approaches for high-performance FPGA applications.

B Design and implement a complete sophisticated digital system application on an FPGA.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to translate a software application into hardware logic for FPGA architectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to understand design synthesizable VHDL systems based on industry-standard coding methods</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand optimize logic for various performance goals (timing, frequency, area, and power).</td>
</tr>
</tbody>
</table>

Unit I
Introduction to Asics, CMOS Logic and ASIC Library Design Types of ASICs - Design Flow - CMOS transistors, CMOS design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - transistors as resistors - transistor parasitic capacitance - Logical effort - Library cell design - Library architecture

Unit II
Programmable Logic Cells and I/O Cells Digital clock Managers-Clock management-Regional clocks- Block RAM – Distributed RAM Configurable Logic Blocks-LUT based structures – Phase locked loops- Select I/O resources –Anti fuse - static RAM - EPROM and EEPROM technology.

Unit III
Device Architectures Device Architecture-Spartan 6 -Vertex 4 architecture- Altera Cyclone and Quartos architectures

Unit IV
Unit V
Floor Planning, Placement and Routing System partition - FPGA partitioning - partitioning methods - floor planning - placement

Unit VI
Physical design flow - global routing - detailed routing - special routing - circuit extraction – DRC

TEXT/REFERENCE BOOKS
3. Design manuals of Altera, Xilinx and Actel.
ELECTIVE IV
NANOSCALE DEVICES AND CIRCUIT DESIGN

Weekly Teaching Hours  TH : 03  Tut: --
Scheme of Marking    TH :60  Tests : 20  IA: 20  Total : 100

Course Objective:

<table>
<thead>
<tr>
<th></th>
<th>To provide knowledge of device physics/operation, technologies and issues in nanoscale CMOS and other emerging devices.</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>Developing innovative circuit design and integration technologies using nanostructured materials</td>
</tr>
<tr>
<td>C</td>
<td>The student will have the knowledge of silicon technology scaling and trends</td>
</tr>
<tr>
<td>D</td>
<td>The student will have the knowledge of challenges of technology scaling in nano-scale regimes</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th></th>
<th>Learner will be able to exploiting non-classical cmos devices for circuit Design in such technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to acquire knowledge of prospects of future non-silicon nanotechnologies</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to acquire knowledge of challenges associated leakage currents and process variations</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to develop a new design techniques under excessive Leakage and process variations</td>
</tr>
</tbody>
</table>

UNIT I
CMOS scaling challenges in Nano scale regimes: Moor and Koomey's law, Leakage current mechanisms in Nano scale CMOS, leakage control and reduction techniques, process variations in devices and interconnects.

UNIT II
Device and technologies for sub 100nm CMOS: Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate;

UNIT III
Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

UNIT IV
Device scaling and ballistic MOSFET: Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in
MOSFETs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs

**UNIT V**
Emerging Nano scale devices: Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, Tunnel FET, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

**UNIT IV**
Non-classical CMOS: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

**TEXT/REFERENCE BOOKS**
3. Hanson, G.W., Fundamentals of Nanoelectronics, Pearson India. 2008
6. Research and Review papers in specific area
ELECTIVE-IV
ANALYSIS AND DESIGN OF DIGITAL SYSTEMS USING VHDL

Weekly Teaching Hours TH : 03 Tut: --
Scheme of Marking TH : 60 Tests : 20 IA: 20 Total : 100

Course Objective:

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<tbody>
<tr>
<td>A</td>
<td>To prepare the student to understand the VHDL language feature to realize the complex digital systems.</td>
</tr>
<tr>
<td>B</td>
<td>To design and simulate sequential and concurrent techniques in VHDL</td>
</tr>
<tr>
<td>C</td>
<td>To explain modeling of digital systems using VHDL and design methodology</td>
</tr>
<tr>
<td>D</td>
<td>To explain predefined attributes and configurations of VHDL.</td>
</tr>
<tr>
<td>E</td>
<td>To Understand behavioral, non-synthesizable VHDL and its role in modern design</td>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to demonstrate, simulate, verify, and synthesize with hardware description languages.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to design digital logic circuits in different types of modeling</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to demonstrate timing and resource usage associated with modeling approach.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to use computer-aided design tools for design of complex digital logic circuits.</td>
</tr>
</tbody>
</table>

UNIT I

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

UNIT II

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

UNIT III

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.
UNIT IV
Data flow and behavioral description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioral description of hardware.

UNIT V
CPU modeling for discrete design- Parwan CPU, behavioral description, bussing structure, data flow, test bench, a more realistic Parwan.

UNIT VI
Interface design and modeling. VHDL as a modeling language.

TEXTBOOKS / REFERENCE:

3. Z. Navabi,”VHDL: modular design and synthesis of cores and systems”, McGraw
5. Recent literature in Analysis and Design of Digital Systems using VHDL.
ELECTIVE V
ASIC AND SOC

Weekly Teaching Hours
TH : 03    Tut: --

Scheme of Marking
TH :60    Tests : 20   IA: 20   Total : 100

Course Objective:

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<tbody>
<tr>
<td>A</td>
<td>Impart the knowledge and skills for RTL (Register Transfer Level) designing and netlist generation</td>
</tr>
<tr>
<td>B</td>
<td>The learning encompasses SOC designing and also focuses on HDL techniques for high performance designs intended for programmable logic devices.</td>
</tr>
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</table>

Course Outcomes:

<table>
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<tbody>
<tr>
<td>CO1</td>
<td>Understand the fundamentals of logic designing and Analog/Mixed signal (AMS) IC designing</td>
</tr>
<tr>
<td>CO2</td>
<td>Perform ASIC verification</td>
</tr>
<tr>
<td>CO3</td>
<td>Conduct design Synthesis for ASIC methodologies</td>
</tr>
<tr>
<td>CO4</td>
<td>Demonstrate high performance designs using HDL techniques</td>
</tr>
</tbody>
</table>

Unit I
Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

Unit II
ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC, ASIC Construction – Floor planning & placement – Routing

Unit III

Unit IV

Unit V
Verification Strategy On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies. MPSoCs. Techniques for designing MPSoCs
Unit VI

SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.

TEXT BOOKS / REFERENCE:

ELECTIVE V
IC TECHNOLOGY

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

A  This course introduces students to the fundamentals of VLSI manufacturing processes and technology.

Course Outcome:

<table>
<thead>
<tr>
<th>CO1</th>
<th>To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.</th>
</tr>
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<tbody>
<tr>
<td>CO2</td>
<td>To learning lithography techniques and concepts of wafer exposure system, types of resists etc.</td>
</tr>
<tr>
<td>CO3</td>
<td>To understand concepts of thermal oxidation and Si/SiO2 interface and its quality measurements.</td>
</tr>
<tr>
<td>CO4</td>
<td>To learn concepts of thin film deposition including chemical Vapor Deposition and Physical vapor deposition.</td>
</tr>
<tr>
<td>CO5</td>
<td>To understand back-end technology to define contacts, interconnect, gates, source and drain, and measurement techniques to insure quality of designs.</td>
</tr>
<tr>
<td>CO6</td>
<td>To understand MOS and Bipolar Process Integration.</td>
</tr>
</tbody>
</table>

UNIT I
Introduction
Introduction to Semiconductor Manufacturing and fabrication. Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.

UNIT II
Lithography, Thermal Oxidation of Silicon:

UNIT III
Diffusion, Ion Implantation Film Deposition:
The Diffusion Process, Mathematical Model for Diffusion, Constant-, The Diffusion Coefficient, Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice
Damage and Annealing, Shallow Implantations, Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy.

**UNIT IV**
Interconnections and Contacts, Packaging and Yield Metal Interconnections and Contact Technology, Diffused Interconnections, Polysilicon Interconnections and Buried Contacts, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.

**UNIT V**
MOS Process Integration, Bipolar Process Integration, Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology, The Junction-Isolated Structure, Current Gain, Transit Time, Basewidth, Breakdown Voltages, Other Elements In SBC Technology

**UNIT VI**

**TEXT BOOKS / REFERENCE:**
Elective V
LINEAR ALGEBRA

Weekly Teaching Hours
TH : 03   Tut: --

Scheme of Marking
TH : 60   Tests : 20   IA: 20   Total : 100

Course Objectives:

| A | To provide in-depth understanding of fundamental concepts of linear algebra |
| B | To understand the importance of linear algebra and learn its applicability to practical problems |

Course Outcomes:

| CO1 | Student will learn to solve and analyze linear system of equation |
| CO2 | Student will analyze the direct notations, duality, adjointness, bases, dual bases in linear algebra |
| CO3 | Student will understand the concept of Linear transformations and matrices, equivalence, similarity. |
| CO4 | Student will be able to find eigen values and eigen vectors using characteristics polynomials |
| CO5 | Student will learn to find the singular value decomposition of the matrix |
| CO6 | Student will be to find the inverse of matrix |

UNIT I
Fields Fq, R, C. Vector Spaces over a field, Fn, F[x]=Polynomials in one Variable.

UNIT II
Direct Notations, Ket, bra vector, duality, adjointness, linear transformations, bases, dual bases.

UNIT III
Linear transformations and matrices, equivalence, similarity.

UNIT IV
Eigenvalues, eigenvectors, diagonalization, Jordancanonical form

UNIT V
Bilinear and sesquilinear forms, inner product, orthonormal, bases, orthogonal decomposition, projections

UNIT VI
System of equations, generalized inverses.
TEXT BOOKS / REFERENCE:
ELECTIVE V
RESEARCH METHODOLOGY

Weekly Teaching Hours

| TH : 03 | Tut:  -- |

Scheme of Marking

| TH :60 | Tests : 20 | IA: 20 | Total : 100 |

Course Objectives:

| A | To develop a research orientation among the scholars and to acquaint them with fundamentals of research methods. |
| B | To develop understanding of the basic framework of research process. |
| C | To identify various sources of information for literature review and data collection. |
| D | To understand the components of scholarly writing and evaluate its quality. |

Course Outcomes:

| CO1 | Student will learn the meaning, objective, motivation and type of research |
| CO2 | Student will be able to formulate their research work with the help of literature review |
| CO3 | Student will be able to develop an understanding of various research design and techniques |
| CO4 | Student will have an overview knowledge of modeling and simulation of research work |
| CO5 | Student will be able to collect the statistical data with different methods related to research work |
| CO6 | Student will be able to write their own research work with ethics and non-plagiarized way |

UNIT I
Introduction: Defining research, Motivation and Course Objective:s, Types of research
Meaning of Research, Course Objective:s of Research, Motivation in Research, Types of Research

UNIT II
Research Formulation: Formulating The research Problem, Literature Review, Development of Working Hypothesis

UNIT III

UNIT IV
Overview of Modeling and Simulation: Classification of models, Development of Models, Experimentation, Simulation.

UNIT V
Statistical Aspects: Methods of Data Collection, Sampling Methods, Statistical analysis, Hypothesis testing.

UNIT VI

TEXT BOOKS / REFERENCE:
1. J.P. Holman, Experimental Methods for Engineers
2. C.R. Kothari, Research Methodology, Methods & Techniques
Course Objectives:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>Students will be explored to the interconnection and integration of the physical world and the cyber space.</td>
</tr>
<tr>
<td>B</td>
<td>To provide ability to design and develop IOT devices.</td>
</tr>
</tbody>
</table>

Course Outcomes:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand the meaning of internet in general and IOT in terms of layers, protocols, packets peer to peer communication.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to interpret IOT working at transport layer with the help of various protocols.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand IOT concept at data link layer.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to apply the concept of mobile networking to the internet connected devices.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to measure and schedule the performance of networked devices in IOT.</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to analyze the challenges involve in developing IOT architecture.</td>
</tr>
</tbody>
</table>

UNIT I

Introduction: What is the Internet of Things: History of IoT, about objects/things in the IoT, Overview and motivations, Examples of applications, IoT definitions, IoT Frame work, General observations, ITU-T views, working definitions, and basic nodal capabilities.

UNIT II

Fundamental IoT Mechanisms & Key Technologies : Identification of IoT objects and services, Structural aspects of the IoT, Environment characteristics, Traffic characteristics ,scalability, Interoperability, Security and Privacy, Open architecture, Key IoT Technologies ,Device Intelligence, Communication capabilities, Mobility support, Device Power, Sensor Technology, RFID technology, Satellite Technology.

UNIT III


UNIT IV

Wireless Technologies For IoT : Layer ½ Connectivity : WPAN Technologies for IoT/M2M, Zigbee /IEEE 802.15.4, Radio Frequency for consumer Electronics ( RF4CE), Bluetooth and
its low-energy profile, IEEE 802.15.6 WBANS, IEEE 802.15 WPAN TG4j, MBANS, NFC, dedicated short range communication (DSRC) & related protocols. Comparison of WPAN technologies cellular & mobile network technologies for IoT/M2M.

UNIT V


UNIT VI

Internet of Things Application Examples: Smart Metering, advanced metering infrastructure, e-Health/Body area network, City automation, automotive applications. Home automation, smart cards, Tracking, Over-The-Air passive surveillance/Ring of steel, Control application examples.

TEXTBOOKS / REFERENCE:

2. Daniel Minoli, Building the Internet of Things with IPv6 and MIPv6 The Evolving World of M2M Communications, Wiley Publications
**SEMINAR I**

<table>
<thead>
<tr>
<th>Weekly Teaching Hours</th>
<th>TH: -</th>
<th>Practical: 04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme of Marking</td>
<td>IA: 50</td>
<td>PR/OR: 50</td>
</tr>
</tbody>
</table>

The seminar shall be on the state of the art in the area of the wireless communication and computing and of student’s choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.
### MINI PROJECT

<table>
<thead>
<tr>
<th>Weekly Teaching Hours</th>
<th>TH: -</th>
<th>Practical: 04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme of Marking</td>
<td>IA: 50</td>
<td>PR/OR: 50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total: 100</td>
</tr>
</tbody>
</table>

The mini project shall be based on the recent trends in the industry, research and open problems from the industry and society. This may include mathematical analysis, modelling, simulation, and hardware implementation of the problem identified. The mini project shall be of the student’s choice and approved by the guide. The student has to submit the report of the work carried out in the prescribed format signed by the guide and head of the department/institute.
The Student has to choose this course either from NPTEL/MOOCs/SWAYAM pool. It is mandatory to get the certification of the prescribed course.
Project-I is an integral part of the final project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation that may include mathematical model/SRS/UML/ERD/block diagram/ PERT chart, and layout and design of the proposed system/work. As a part of the progress report of project-I work, the candidate shall deliver a presentation on progress of the work on the selected dissertation topic. It is desired to publish the paper on the state of the art on the chosen topic in international conference/journal. The student shall submit the duly certified progress report of project-I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.
**PROJECT-II**

<table>
<thead>
<tr>
<th>Weekly Teaching Hours</th>
<th>TH: -</th>
<th>Practical: -</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme of Marking</td>
<td>IA: 100</td>
<td>PR/OR: 100</td>
</tr>
</tbody>
</table>

In Project - II, the student shall complete the remaining part of the project which will consist of the simulation/ analysis/ synthesis/ implementation / fabrication of the proposed project work, work station, conducting experiments and taking results, analysis and validation of results and drawing conclusions.

It is mandatory to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.