Dr. Babasaheb Ambedkar Technological University

Course Structure and Syllabus

For

M. Tech. (VLSI and Embedded System)

Two Year (Four Semester) Course

(w.e.f. July 2017)

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,

Lonere-402103, Raigad (MS)

M.Tech. (VLSI and Embedded System)

Objectives:

I. To serve the society and nation, by providing high quality engineering educational programs to the students, engaging in research and innovations that will enhance the skill and knowledge and assisting the economic development of the region, state, and nation through technology transfer.

II. To equip the postgraduate students with the state of the art education through research and collaborative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.

III. To encourage the post-graduates students, to acquire the academic excellence and skills necessary to work as Electronics and Telecommunication professional in a modern, ever-evolving world.

IV. To provide the broad understanding of social, ethical and professional issues of contemporary engineering practice and related technologies, as well as professional, ethical, and societal responsibilities.

V. To inculcate the skills for perusing inventive concept to provide solutions to industrial, social or nation problem.

Outcomes:

I. Students of this program will have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.

II. Postgraduate students will gain an ability to design and conduct experiments, as well as to analyze and interpret data/results.

III. Learners of this program will built an ability to design and develop a system, components, devices, or process to meet desired needs.

IV. Masters students of this program will have an ability to work on multi-disciplinary teams and also as an individual for solving issues related to Electronics and Telecommunication.

V. Learners of this program will have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

VI. Postgraduate students will have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.

VII. Postgraduate students will have an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.

VIII. Learners of this program will have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, and user friendliness to cater needs for innovative product development.

IX. Postgraduate students will have an ability to solve contemporary social and industrial problems by engaging in life-long learning.

Dr. Babasaheb Ambedkar Technological University

Revised Teaching and Examination Scheme for
M.Tech. (VLSI and Embedded System) w.e.f. July 2017

Sr. No.	Course Code	Name of the Course	Hours/Week			Credit	Examination scheme				
							Theory		IA	PR/OR	TOTAL
			L	P	T		TH	Test			
First Semester											
01	MTVEC101	VLSI Technology and Design	03	--	1	04	60	20	20	--	**100**
02	MTVEC102	CMOS Analog Circuit Design	03	--	1	04	60	20	20	--	**100**
03	MTVEC103	Advanced Embedded Logic	03	--	1	04	60	20	20	--	**100**
04	MTVEE114	Elective-I	03	--	--	03	60	20	20	--	**100**
05	MTVEE125	Elective-II	03	--	--	03	60	20	20	--	**100**
06	MTVEC106	Communication Skills	02	--	--	02	--	--	25	25	**50**
07	MTVEL107	PG Lab-I(VLSI Laboratory)*	--	03	--	02	--	--	25	25	**50**
		Total for Semester I	**17**	**03**	**03**	**22**	**300**	**100**	**150**	**50**	**600**
Second Semester											
01	MTVEC201	Embedded Real Time Operating Systems	03	--	1	04	60	20	20	--	**100**
02	MTVEC202	CMOS Mixed Signal Circuit Design	03	--	1	04	60	20	20	--	**100**
03	MTVEE233	Elective-III	03	--	--	03	60	20	20	--	**100**
04	MTVEE244	Elective- IV	03	--	--	03	60	20	20	--	**100**
05	MTVEE255	Elective-V- (Open to all)	03	--	--	03	60	20	20	--	**100**
06	MTVES206	Seminar-I	--	04	--	02	--	--	50	50	**100**
07	MTVEP207	Mini-Project	--	04	--	02	--	--	50	50	**100**
		Total for Semester II	**15**	**8**	**02**	**21**	**300**	**100**	**200**	**100**	**700**
Third Semester											
1	MTVEC301	Project Management & Intellectual Property Rights (Self Study)#	--	--	--	02	--	--	50	50	**100**
2	MTVEP302	Project-I	--	--	--	10	--	--	50	50	**100**
		Total for Semester III	**--**	**--**	**-**	**12**	**--**	**--**	**100**	**100**	**200**
Fourth Semester											
1	MTVEP401	Project-II	--	--	--	20	--	--	100	100	**200**
		Total for Semester IV	**--**	**--**	**--**	**20**	**--**	**--**	**100**	**100**	**200**
GRAND TOTAL											**1700**

* PG Lab-I –Practical shall be based on courses of first semester.

\# Student has to choose this course either from NPTEL/MOOC pool and submission of course completion certificate is mandatory.

Elective-I
    A. Hardware Software Co-Design
    B. Digital System Design
    C. Soft Computing Techniques
    D. CPLD and FPGA Architectures and Applications
    E. Advanced Computer Architecture

Elective-II
    A. Advanced Operating Systems
    B. Network Security and Cryptography
    C. CMOS Digital Integrated Circuit Design
    D. Embedded C
    E. Optical Communication Design & Test

Elective-III
    A. Design for Testability
    B. Digital Signal Processors and Architectures
    C. System On Chip Architecture
    D. Embedded Networking
    E. RF Circuit Design

Elective-IV
    A. Sensors and Actuators
    B. Low Power VLSI Design
    C. Semiconductor Memory Design and Testing
    D. Analog and Mixed Signal Processing
    E. Analysis and Design of Digital Systems using VHDL

Elective-V (Open)
    A. Internet of Things
    B. Linear Algebra
    C. Neural Networks in Embedded Applications
    D. Research Methodology
    E. Wavelet Transforms and its Applications

VLSI TECHNOLOGY AND DESIGN

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To introduce MOS technology and its layout design rules
B	To provide basic knowledge sequential and combinational logic design

Course Outcomes:

CO1	Learner will be able to express technologies such as MOS, BiCMOS
CO2	Learner will get knowledge of design tools for CMOS
CO3	Learner will be able to design basic gates and their alternative circuits
CO4	Learner will be able to design and simulate combinational logic designs
CO5	Learner will be able to validate and test the design

UNIT I

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids − Vds relationships, Threshold Voltage V_T, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT III

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT IV

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing

UNIT V

Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

Textbooks / References:

1. K. Eshraghian Eshraghian. D, A. Pucknell, Essentials of VLSI Circuits and Systems, , 2005, PHI.   2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.
2. Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective –CRC Press, 2011.
3. N.H.E Weste, K. Eshraghian, Principals of CMOS VLSI Design –, 2nd Ed., Addison Wesley.

CMOS ANALOG CIRCUIT DESIGN

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To introduce modeling/design of different circuits using CMOS

Course Outcomes:

CO1	Learner will be able to express modeling of passive components
CO2	Learner will be able to interpret modeling parameters
CO3	Learner will be able to differentiate learn different architectures of CMOS amplifier
CO4	Learner will be able to design multistage CMOS operational amplifier
CO5	Learner will be able to characterize comparators

UNIT I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout.

UNIT II

CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT III

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT IV

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT V

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT VI

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks / References:

1. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design - Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits- Wiley India, Fifth Edition, 2010.
3. David A. Johns, Ken Martin, Analog Integrated Circuit Design- Wiley Student Edn, 2013.
4. Behzad Razavi, Design of Analog CMOS Integrated Circuits- TMH Edition.
5. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

ADVANCED EMBEDDED LOGIC

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To introduce ARM architecture
B	Use of VHDL for modeling and simulation
C	Basic concept of android OS

Course Outcomes:

CO1	Learner will be able to list ARM instruction set
CO2	Learner will be able to interface I/O devices with ARM
CO3	Learner will be able to design, debug and simulate practical examples
CO4	Learner will be able to identify fault in the system
CO5	Learner will be have knowledge of different operating systems

UNIT I

The ARM architecture, ARM organization and implementation, The ARM instruction set, The thumb instruction set, Basic ARM Assembly language program, ARM CPU cores.

UNIT II

Interfacing Memory and I/O devices, synchronous and asynchronous transfer, DMA, Serial data transfer, GPIB, RS-232C, I2C, CAN bus protocols. RFID, Smartcards, PDA's, Zip drives.

UNIT III

Host and target machines, Linkers / Locators for Embedded Software, Debugging techniques Instruction set simulators, Practical example– Source code.

UNIT IV

Hardware description languages - VHDL and Verilog, programming and subsystem design concepts, Fault Modeling and Simulation, Functional testing, Design for testability, Scan based designs, Boundary scan standards (JTAG), BIST, BILBO

UNIT V

Tasks and Task states, Semaphores, Shared data, Message queues, Interrupt routines – Encapsulating semaphore and queues, Hard Real-time scheduling, Power saving.

UNIT VI

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Textbooks / References:

1. David. E.Simon, "An Embedded Software Primer", Pearson Education, 2001.
2. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
3. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004
4. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
5. Steave Furber, "ARM system – on – chip architecture", Addison Wesley, 2000
6. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
7. VHDL: D. Perry,MaGraw Hill Int. Edition.
8. Advanced UNIX Programming, Richard Stevens.
9. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

HARDWARE - SOFTWARE CO-DESIGN

Weekly Teaching Hours	TH : 03	Tut:	01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100	

Course Objectives:

A	Show benefits of the codesign approach over current design process
B	Illustrate how codesign concepts are being introduced into design methodologies
C	Introduce the fundamentals of HW/SW codesign and partitioning concepts in designing embedded systems

Course Outcomes:

CO1	Learner will be able to express co-design issues
CO2	Learner will have knowledge of Prototyping and emulation techniques
CO3	Learner will have knowledge of Architecture Specialization techniques
CO4	Learner will have knowledge of Tools for Embedded Processor Architectures
CO5	Learner will be able to design and verify computational models

UNIT I

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT III

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT IV

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT VI

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Textbooks / References:

1. Jorgen Staunstrup, Wayne Wolf Hardware / Software Co- Design Principles and Practice — 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, Hardware / Software Co- Design - 2002, Kluwer Academic Publishers
3. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Co-design - 2010 – Springer

DIGITAL SYSTEM DESIGN

Weekly Teaching Hours	TH : 03	Tut: --			
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100	

Course Objective:

A	To get an idea about designing complex, high speed digital systems and how to implement such design

Course Outcomes:

CO1	Learner will be able to identify mapping algorithms into architectures.
CO2	Learner will be able to understand various delays in combinational circuit and its optimization methods.
CO3	Learner will be able to understand circuit design of latches and flip-flops
CO4	Learner will be able to demonstrate combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5	Learner will be able to understand the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.

UNIT I

Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

UNIT II

Combinational network delay. Power and energy optimization in combinational logic circuit.

Sequential machine design styles. Rules for clocking. Performance analysis.

UNIT III

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

UNIT IV

Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division.

UNIT V

SRAM, DRAM, ROM, serial access memory, context addressable memory.

UNIT VI

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures-Single context, Multi context, partially reconfigurable, Pipeline reconfigurable,

Block Configurable, Parallel processing.

Textbooks / References:

1. N. H.E.Weste, D. Harris, CMOS VLSI Design (3/e), Pearson, 2005.
2. W.Wolf, FPGA- based System Design, Pearson, 2004.
3. S.Hauck, A.DeHon, Reconfigurable computing: the theory and practice of FPGA-basedcomputation, Elsevier, 2008.
4. F.P. Prosser, D. E. Winkel, Art of Digital Design, 1987.
5. R.F.Tinde, Engineering Digital Design, (2/e), Academic Press, 2000.
A. Bobda, Introduction to reconfigurable computing, Springer, 2007.
6. M.Gokhale, P.S.Graham, Reconfigurable computing: accelerating computation with field-programmable gate arrays, Springer, 2005.
7. C.Roth, Fundamentals of Digital Logic Design, Jaico Publishers, V ed., 2009.
8. Recent literature in Digital System Design.

SOFT COMPUTING TECHNIQUES

Weekly Teaching Hours	TH: 03	Tut: 01		
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

A	To expose the concepts of feed forward neural networks.
B	To provide adequate knowledge about feedback neural networks.
C	To teach about the concept of fuzziness involved in various systems.
D	To expose the ideas about genetic algorithm
E	To provide adequate knowledge about of FLC and NN toolbox

Course Outcomes:

CO1	Learner will be familiar with the concept of artificial neural network
CO2	Learner will be able to model fuzzy logic operations
CO3	Learner will be able to solve typical control problems using genetic algorithm
CO4	Learner will be able to identify and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox
CO5	Learner will be able to Implement of fuzzy logic controller using MATLAB fuzzy-logic toolbox

UNIT I

Introduction:

Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rulebased systems, the AI approach, Knowledge representation - Expert systems.

UNIT II

Artificial Neural Networks:

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT III

Fuzzy Logic System:

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT IV

Genetic Algorithm:

Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT V

Applications I:

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox,

UNIT VI

Applications II:

Stability analysis of Neural Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

Textbooks / References:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.
3. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.
4. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
5. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
6. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
7. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.
8. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.
9. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Weekly Teaching Hours	TH: 03	Tut: 01		
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To introduce field programmable logic devices and their design applications

Course Outcomes:

CO1	Learner will acquire Knowledge about various architectures and device technologies of PLD's
CO2	Learner will be able to Comprehend FPGA Architectures.
CO3	Learner will be able to analyze System level Design and their application for Combinational and Sequential Circuits.
CO4	Learner will be familiar with Anti-Fuse Programmed FPGAs
CO5	Learner will able to apply knowledge of this subject for various design applicaitons

UNIT I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator,

UNIT VI

A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Textbooks / References:

1. Stephen M. Trimberger, Field Programmable Gate Array Technology - Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, Digital Systems Design - Cengage Learning.
3. John V. Oldfield, Richard C. Dorf, Field Programmable Gate Arrays - Wiley India.
4. Pak K. Chan/Samiha Mourad, Digital Design Using Field Programmable Gate Arrays - Pearson Low Price Edition.
5. Ian Grout, Digital Systems Design with FPGAs and CPLDs - Elsevier, Newnes.
6. Wayne Wolf, FPGA based System Design - Prentice Hall Modern Semiconductor Design Series.

ADVANCED COMPUTER ARCHITECTURE

Weekly Teaching Hours	TH: 03	Tut: --		
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	The objective of this course is to learn the fundamental aspects of computer architecture design and analysis.

Course Outcomes:

CO1	Learner will be able to understand different processor architectures and system-level design processes.
CO2	Learner will be able to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design
CO3	Learner will be able to understand the principles of I/O in computer systems, including viable mechanisms for I/O and secondary storage organization.
CO4	Learner will be able to understand basic concept of pipelining
CO5	Learner will be able to understand Multiprocessor architecture
CO6	Learner will be able to understand Non von Neumann Architectures

UNIT I

Overview of von Neumann architecture: Instruction set architecture; The Arithmetic and Logic Unit, The Control Unit, Memory and I/O devices and their interfacing to the CPU; Measuring and reporting performance; CISC and RISC processors.

UNIT II

Pipelining: Basic concepts of pipelining, data hazards, control hazards, and structural hazards; Techniques for overcoming or reducing the effects of various hazards.

UNIT III

Hierarchical Memory Technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies..

UNIT IV

Instruction-level parallelism: Concepts of instruction-level parallelism (ILP), Techniques for increasing ILP; Superscalar, superpipelined and VLIW processor architectures; Vector and symbolic processors; Case studies of contemporary microprocessors.

UNIT V

Multiprocessor Architecture: Taxonomy of parallel architectures; Centralized shared-memory architecture, synchronization, memory consistency, interconnection networks; Distributed shared-memory architecture, Cluster computers.

UNIT VI

Non von Neumann Architectures: Data flow Computers, Reduction computer architectures, Systolic Architectures.

Textbooks / References:
1. W. Stallings, Computer Organization and Architecture: Designing for performance, 4th Ed. PHI, 1996.
2. J. H. Hennessy and D. A. Patterson, Computer Architecture: A Quantitative Approach, 2nd Ed., Morgan Kaufmann, 1996.
3. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability and Programmability McGraw-Hill Inc, 1993.
4. D. E. Culler, J. Pal Singh, and A. Gupta, Parallel Computer Architecture: A Hardware/Software Approach, Harcourt Asia Pte Ltd., 1999.

ELECTIVE II

ADVANCED OPERATING SYSTEMS

Weekly Teaching Hours	TH: 03	Tut: 01		
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

A	To learn the basic and advanced concepts of operating systems.

Course Outcomes:

CO1	students will understand how the operating system defines an abstraction of hardware behavior with which programmers can control the hardware.
CO2	students will understand how operating system manages resource sharing among the computer's users
CO3	Learner will know basic commands and command arguments for UNiX and LINUX
CO4	Learner will have knowledge of distributed systems
CO5	Learner will be able to detect and prevent deadlock in distributed system

UNIT I

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT II

Introduction to UNIX and LINUX: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT III

System Calls: System calls and related file structures, Input / Output, Process creation & termination. Inter Process **Communication:** Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication**.**

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

UNIT VI

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Textbooks / References:

1. Maurice J. Bach, The Design of the UNIX Operating Systems –1986, PHI.
2. Andrew. S. Tanenbaum, Distributed Operating System 1994, PHI.
3. Richard Peterson, The Complete Reference LINUX – 4th Ed., McGraw – Hill.
4. Stallings, Operating Systems: Internal and Design Principles - 6th Ed., PE.
5. Andrew S Tanenbaum,Modern Operating Systems - 3rd Ed., PE.
6. Abraham Silberchatz, Peter B. Galvin, Greg Gagne, Operating System Principles - 7th Ed., John Wiley 4. UNIX User Guide – Ritchie & Yates.
7. W.Richard Stevens,UNIX Network Programming - 1998, PHI.

NETWORK SECURITY AND CRYPTOGRAPHY

Weekly Teaching Hours	TH: 03	Tut: 01		
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To understand OSI security architecture and classical encryption techniques
B	Describe the principles of public key cryptosystems, hash function and digital signature

Course Outcomes:

CO1	Learner will get knowledge of various classical techniques for encription
CO2	Learner will be able to compare various cryptographic techniques
CO3	Learner will be able to design secure application
CO4	Learner will be able to inject secure coding in developed application

UNIT I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT III

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT IV

Hash and Mac Algorithms: MD File, Message digests Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service.

Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management**.**

Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

UNIT VI

Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

Textbooks / References:

1. William Stallings, Cryptography and Network Security: Principles and Practice - 2000, PE.
2. Mark Burgess,John Wiel, Principles of Network and Systems Administration

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To create model of moderately sized CMOS circuits that realize specified digital functions
B	Have an understanding of the characteristics of CMOS circuit construction

Course Outcomes:

CO1	Learner will be familiar with basic MOS characteristics
CO2	Learner will be able to design CMOS logic gates
CO3	Learner will be able to model complex combinational logic circuits
CO4	Learner will be able to realize sequential MOS logic circuits
CO5	Learner will have knowledge of various types of semiconductor memories

UNIT I

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate,

UNIT III

Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT IV

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT V

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Textbooks / References:

1. Ken Martin, Digital Integrated Circuit Design –Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design –TMH, 3rd Ed., 2011.
3. Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective –CRC Press, 2011
4. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits – A Design Perspective, 2nd Ed., PHI.

EMBEDDED C

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To understand role of programming language in embedded systems

Course Outcomes:

CO1	Learner will be able to define embedded system
CO2	Learner will be able to classify between processors, programming languages, operating systems etc.
CO3	Learner will be able to describe architecture of 8051 microcontroller
CO4	Learner will be able to write a program basic techniques for reading from port pins
CO5	Learner will learn concept of Object oriented programming
CO6	Learner will be able to create hardware delays using timers
CO7	Learner will be able to solve a real word problem using knowledge of embedded C

UNIT I

Programming Embedded Systems in C

Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

UNIT II

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT III

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT IV

Adding Structure to the Code

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT V

Meeting Real-Time Constraints

Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT VI

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

Textbooks / References:

1. Michael J. Pont , Embedded C, A Pearson Education
2. Nigel Gardner, PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C

OPTICAL COMMUNICATION DESIGN AND TEST

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To understand optics phenomenon.
B	To know basics of lenses and their types.

Course Outcomes:

CO1	Learner will be able to understand concept of aberrations.
CO2	Learner will be able to perform image evaluation.
CO3	Learner will be able to classify types of lenses.
CO4	Learner will be able to understand basic of optics.
CO5	Learner will be able to understand optimization techniques in lens design.
CO6	Learner will be able to get familiar with telescope.

UNIT I

Aberrations: Transverse ray and wave aberrations, chromatic aberration; Ray tracing: paraxial, finite and oblique rays

UNIT II

Image evaluation: transfer functions, point spread function, encircled energy and its computation and measurement, optimization techniques in lens design, merit function, damped least square methods, orthonormalization, and global search method, Tolerance analysis.

UNIT III

Achromatic doublets, achromats and aplanats; Cooke triplet and its derivatives.

UNIT IV

Double Gauss lens, Zoom lenses and aspherics, GRIN optics, focal shift, high and low N number focusing systems, focusing of light in stratified media, high numerical aperture focusing, basics of non-paraxial propagation of light.

UNIT V

Classification of lens systems. Refractive systems- cookes triplet, Gatelecentric system, telephoto system, f-theta lens (fish eye lens).

UNIT VI

Relective systems–single mirror telescope, two mirror telescope–Greogrian, dall-kirkham, marsenne, cassegrain, R-C telescope, three mirror aspheric system: unobscured system, obscured system.

Textbooks / References:

1. A. C. Kak and Malcolm Slaney, Principles of Computerized Tomographic Imaging. -. IEEE Press
2. Lihong V. Wang and Hsin-i Wu, Biomedical Optics: Principles and Imaging. - Wiley-Interscience.
3. P. Gibson, J. C. Hebden, and S. R. Arridge, Recent advances in diffuse optical imaging, Physics in Medicine and Biology, 50, R1-R43. (2005).
4. S.R.Arridge   Optical tomography in medical imaging, Inverse Problems, 15, R41–R93. (1999)
5. J. W. Goodman, Introduction to Fourier Optics
6. L. Nikolova & P.S. Ramanujam, Polarization holography
7. P. Hariharan, Optical holography principles techniques and applications

COMMUNICATION SKILLS

Weekly Teaching Hours	TH: 02		Practical: -	
Scheme of Marking	TH: --	IA: 25	PR/OR: 25	Total: 50

Course Objective:

A	To become more effective confident speakers and deliver persuasive presentations
B	To develop greater awareness and sensitivity to some important considerations in interpersonal communication and learn techniques to ensure smoother interpersonal relations

Course Outcomes:

CO1	Learner will be able to understand the fundamental principles of effective business communication
CO2	Learner will be able to apply the critical and creative thinking abilities necessary for effective communication in today's business world
CO3	Learner will be able to organize and express ideas in writing and speaking to produce messages suitably tailored for the topic, objective, audience, communication medium and context
CO4	Learner will be able to demonstrate clarity, precision, conciseness and coherence in your use of language
CO5	Learner will be able to become more effective confident speakers and deliver persuasive presentations

UNIT I

Introduction to communication, Necessity of communication skills, Features of good communication, Speaking skills, Feedback & questioning technique, Objectivity in argument

UNIT II

Verbal and Non-verbal Communication, Use and importance of non-verbal communication while using a language, Study of different pictorial expressions of non-verbal communication and their analysis

UNIT III

Academic writing, Different types of academic writing, Writing Assignments and Research Papers, Writing dissertations and project reports

UNIT IV

Presentation Skills: Designing an effective Presentation, Contents, appearance, themes in a presentation; Tone and Language in a presentation, Role and Importance of different tools for effective presentation

UNIT V

Motivation/ Inspiration: Ability to shape and direct working methods according to self-defined criteria;Ability to think for oneself, Apply oneself to a task independently with self-motivation, Motivation techniques: Motivation techniques based on needs and field situations

UNIT VI

Self-management, Self-evaluation, Self-discipline, Self-criticism, Recognition of one's own limits and deficiencies, dependency etc. Self-awareness, Identifying one's strengths and weaknesses, Planning & Goal setting, Managing self-emotions, ego, pride leadership & Team dynamics

Textbooks / References:

1. Mitra, Barun, Personality Development and Soft Skills, Oxford University Press, 2016.
2. Ramesh, Gopalswamy, The Ace of Soft Skills: Attitude, Communication and Etiquette for Success, Pearson Education, 2013.
3. Covey, Stephen R., Seven Habits of Highly Effective People: Powerful Lessons in Personal Change, Simon and Schuster, 09-Nov-2004
4. Rosenberg Marshall B., Nonviolent Communication: A Language of Life, Puddle Dancer Press, 01-Sep-2003

PG LAB-I

Weekly Teaching Hours	TH: **--**		Practical: 03	
Scheme of Marking	TH: **--**	IA: 25	PR/OR: 25	Total: 50

Practical's of the Lab - I shall be based on the courses of first semester. The lab work shall consists of hands on experiments on the different software and hardware platforms related to the syllabus.

EMBEDDED REAL TIME OPERATING SYSTEMS

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide understanding of the techniques essential to the design and implementation of device drivers and kernel internals of embedded operating systems.
B	To provide the students with an understanding of the aspects of the Real-time systems and Real-time Operating Systems.
C	To provide an understanding of the techniques essential to the design and implementation of real-time embedded systems.

Course Outcomes:

CO1	Learner will understand the Embedded Real Time software that is needed to run embedded systems
CO2	Learner will understand the open source RTOS and their usage.
CO3	Learner will understand the VxWorks RTOS and realtime application programming with it
CO4	Learner will be able to build device driver and kernel internal for Embedded OS & RTOS

UNIT I

Introduction:

Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.)

UNIT II

Real Time Operating Systems

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization,

UNIT III

Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT IV

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT V

Exceptions, Interrupts and Timers Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT VI

Case Studies of RTOS

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Textbooks / References:
1. Qing Li, Elsevier, Real Time Concepts for Embedded Systems , 2011
2. Rajkamal, Embedded Systems- Architecture, Programming and Design, 2007, TMH.
3. Richard Stevens, Advanced UNIX Programming,
4. Dr. Craig Hollabaugh, Embedded Linux: Hardware, Software and Interfacing.

CMOS MIXED SIGNAL CIRCUIT DESIGN

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To know mixed signal circuits like DAC, ADC, PLL etc.
B	To gain knowledge on filter design in mixed signal mode.
C	To acquire knowledge on design different architectures in mixed signal mode.

Course Outcomes:

CO1	Learner will have knowledge of operation of switched capacitor cicuits
CO2	Learner will be able to design a filter network
CO3	Learner will be able to learn topology of PLL network
CO4	Learner will learn Data Converter Fundamentals

UNIT I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits,

UNIT II

Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT III

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT IV

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT V

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT VI

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

Textbooks / References:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits- TMH Edition, 2002
2. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design - Oxford University Press, International Second Edition/Indian Edition, 2010.
3. David A. Johns, Ken Martin, Analog Integrated Circuit Design- Wiley Student Edition, 2013
4. Rudy Van De Plassche, CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Kluwer Academic Publishers, 2003
5. Richard Schreier, Understanding Delta-Sigma Data converters, Wiley Interscience, 2005.
6. R. Jacob Baker, CMOS Mixed-Signal Circuit Design - Wiley Interscience, 2009.

DESIGN FOR TESTABILITY

Weekly Teaching Hours	TH: 03	Tut:	01		
Scheme of Marking	TH: 60	Tests: 20	IA: 20		Total: 100

Course Objectives:

A	The aim of the course is to introduce the student to various techniques which are designed to reduce the amount of input test patterns required to ensure that an acceptable level of fault coverage has been obtained.

Course Outcomes:

CO1	Learner will understand role of testing in VLSI technology
CO2	Learner will have knowledge of fault modeling
CO3	Learner will be able to simulation of circuit for Design, Verification, and Test Evaluation
CO4	Learner will have knowledge of different testability measure

UNIT I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing,

UNIT II

Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT III

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT IV

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT V

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks / References:

1. M.L. Bushnell, V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, Digital Systems and Testable Design - Jaico Publishing House.
3. P.K. Lala, Digital Circuits Testing and Testability - Academic Press.

ELECTIVE III

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Weekly Teaching Hours	TH: 03	Tut: 01			
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100	

Course Objectives:

A	To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors

Course Outcomes:

CO1	Learner will learn the architecture details fixed and floating point DSPs
CO2	Learner will Infer about the control instructions, interrupts, and pipeline operations, memory and buses.
CO3	Learner will illustrate the features of on-chip peripheral devices and its interfacing with real time application devices
CO4	Learner will learn to implement the signal processing algorithms and applications in DSPs
CO5	Learner will learn the architecture of advanced DSPs

UNIT I

Introduction to Digital Signal Processing: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT II

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT VI

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

Textbooks / References:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing –Thomson Publications, 2004.
2. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, A Practical Approach To Digital Signal Processing - New Age International, 2006/2009
3. Woon-Seng Gan, Sen M. Kuo, Embedded Signal Processing with the Micro Signal Architecture Publisher: Wiley-IEEE Press, 2007
4. B. Venkataramani and M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications –2002, TMH.
5. Jonatham Stein, Digital Signal Processing – 2005, John Wiley.
6. Lapsley et al., DSP Processor Fundamentals, Architectures & Features 2000, S. Chand & Co.
7. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
8. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
9. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

ELECTIVE III

SYSTEM ON CHIP

Weekly Teaching Hours	TH: 03	Tut:	--	
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

A	To provide an in-depth understanding of what SoC is and what are the differences between SoC and Embedded System Design.
B	To provide an in-depth understanding of basics of System on Chip and Platform based
C	To provide an in-depth understanding of issues and tools related to SoC design and implementation.

Course Outcomes:

CO1	Learner will be able to interpret nature of hardware and software, its data flow modeling and implementation techniques
CO2	Learner will be able to analyze the micro-programmed architecture of cores and processors
CO3	Learner will be able to demonstrate system on chip design models
CO4	Learner will be able to hypothesize and synthesize working of advanced embedded systems
CO5	Learner will be able to develop design SOC controller
CO6	Learner will be able to design, implement and test SOC model

UNIT I

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD.

UNIT II

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code,

UNIT III

System on Chip, concept, design principles, portable multimedia system, SOC modelling, hardware/software interfaces, synchronization schemes, memory mapped Interfaces, coprocessor interfaces, coprocessor control shell design, data and control design, Programmer‟s model.

UNIT IV

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

UNIT V

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS

UNIT VI

SOC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

Textbooks / References:
1. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer
2. Sanjay Churiwala, SapanGarg , Principles of VLSI RTL Design A Practical Guide, Springer
3. Youn-Long Steve Lin, Essential Issues in SOC Design, Designing Complex Systems-on-Chip, Springer

EMBEDDED NETWORKING

Weekly Teaching Hours	TH: 03	Tut: --		
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

A	Serial and parallel communication protocols
B	Application Development using USB and CAN bus for PIC microcontrollers
C	Application development using Embedded Ethernet for Rabbit processors.
D	Wireless sensor network communication protocols.

Course Outcomes:

CO1	Learner will be able to get knowledge in the Protocols, Network Related Application
CO2	Learner will be able to have knowledge in USB communication
CO3	Learner will be able to have knowledge of CAN interface/application
CO4	Learner will be able to understand Ethernet basics
CO5	Learner will be able to get knowledge of concept of embedded Ethernet
CO6	Learner will be able to get knowledge of wireless embedded networking

UNIT I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT II

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –

UNIT III

CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT IV

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –

Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT V

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT VI

Wireless Embedded Networking:

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Textbooks / References:
1. Frank Vahid, Tony Givargis, Embedded Systems Design: A Unified Hardware/Software Introduction - John & Wiley Publications, 2002
2. Jan Axelson, Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Penram Publications, 1996.
3. Dogan Ibrahim, Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Elsevier 2008.
4. Jan Axelson, Embedded Ethernet and Internet Complete - Penram publications, 2003.
5. Bhaskar Krishnamachari, Networking Wireless Sensors - Cambridge press 2005.

ELECTIVE-III

RF CIRCUIT DESIGN

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objective:

A	To impart knowledge on basics of IC design at RF frequencies.

Course outcomes

CO1:	Learner will be able to understand the Noise models for passive components and noise theory
CO2:	Learner will be able to analyze the design of a high frequency amplifier
CO3:	Learner will be able to appreciate the different LNA topologies & design techniques
CO4:	Learner will be able to distinguish between different types of mixers
CO5:	Learner will be able to analyse the various types of synthesizers, oscillators and their characteristics.

UNIT I

Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, noise models for active and passive components

UNIT II

High frequency amplifier design – zeros as bandwidth enhancers, shunt-series amplifier, Ft doublers, neutralization and unilateralization

UNIT III

Low noise amplifier design – LNA topologies, power constrained noise optimization, linearity and large signal performance

UNIT IV

Mixers – multiplier-based mixers, subsampling mixers, diode-ring mixers RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.

UNIT V

Oscillators : describing functions, resonators, negative resistance oscillators,

UNIT VI

Synthesizers: synthesis with static moduli, synthesis with dithering moduli, combination synthesizers - phase noise considerations.

Textbooks / References:

1. T.homas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed., Cambridge, UK: Cambridge University Press, 2004.
2. B.Razavi, RF Microelectronics, 2nd Ed., Prentice Hall, 1998.
3. Abidi, P.R. Gray, and R.G. Meyer, eds., Integrated Circuits for Wireless Communications, New York: IEEE Press, 1999.
4. R. Ludwig and P. Bretchko,RF Circuit Design, Theory and Applications, Pearson, 2000.
5. Mattuck,A., Introduction to Analysis, Prentice-Hall,1998.
6. Recent literature in RF Circuits.

SENSORS AND ACTUATORS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	understanding basic laws and phenomena on which operation of sensors and actuators-transformation of energy is based,
B	Conducting experiments in laboratory and industrial environment.

Course Outcomes:

CO1	Learner will be able to characterize types sensors
CO2	Learner will be able to interpret working of different types of sensors
CO3	Learner will be able to describe application of sensor
CO4	Learner will be familiar with Actuation Systems

UNIT I

Sensors / Transducers: Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

UNIT II

Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors

UNIT III

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT IV

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation

UNIT V

Sensors –Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing – Sensors for environmental Monitoring

UNIT VI

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors

Textbooks / References:
1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.
2. W. Bolton – "Mechatronics" –Pearson Education Limited.
3. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

LOW POWER VLSI DESIGN

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To match with todays need for low power circuit design for energy efficient systems

Course Outcomes:

CO1	Learner will be able to classify causes for various power dissipation
CO2	Learner will acquire knowledge of Low-Power Design Approaches
CO3	Lerner will be able to use Switched Capacitance Minimization Approaches
CO4	Learner will be able to design low power adder networks
CO5	Learner will be able to design low power multiplier networks
CO6	Learner will have knowledge of low power memory technologies

UNIT I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

UNIT III

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT IV

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry LookAhead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT V

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, BaughWooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT VI

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks / References:

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits – Analysis and Design –TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, Low-Voltage, Low-Power VLSI Subsystems –TMH Professional Engineering.
3. Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective –CRC Press, 2011
4. Anantha Chandrakasan, Low Power CMOS Design –IEEE Press/Wiley International, 1998.
5. – Kaushik Roy, Sharat C. Prasad, Low Power CMOS VLSI Circuit Design John Wiley & Sons, 2000.
6. Gary K. Yeap, Practical Low Power Digital VLSI Design –Kluwer Academic Press, 2002.
7. A. Bellamour, M. I. Elamasri, Low Power CMOS VLSI Circuit Design –Kluwer Academic Press, 1995.
8. Siva G. Narendran, Anatha Chandrakasan, Leakage in Nanometer CMOS Technologies –Springer, 2005.

SEMICONDUCTOR MEMORY DESIGN AND TESTING

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	In this course the students will learn overview of memory chip design, DRAM circuits performance analysis and design issues Memory Packing Technologies

Course Outcomes:

CO1	Learner will have knowledge of Random Access Memory Technologies
CO2	Learner will have knowledge of Non-volatile Memories
CO3	Learner will have knowledge of Memory Fault Modeling Testing and Memory Design for Testability
CO4	Learner will have knowledge of Semiconductor Memory Reliability
CO5	Learner will have knowledge of Radiation Effects
CO6	Learner will have knowledge of Advanced Memory Technologies

UNIT I

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT IV

Semiconductor Memory Reliability: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification,

UNIT V

Radiation Effects:

Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT VI

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

Textbooks / References:
1. Ashok K. Sharma, Semiconductor Memories Technology 2002, Wiley.
2. Ashok K. Sharma, Advanced Semiconductor Memories – Architecture, Design and Applications - 2002, Wiley.
3. Chenming C Hu, Modern Semiconductor Devices for Integrated Circuits –1st Ed., Prentice Hall.

ELECTIVE IV
ANALOG AND MIXED SIGNAL PROCESSING

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To understand the signal processing concepts of mixed-signal systems.
B	The ability to use this knowledge to design mixed-signal processing systems on system level.

Course Outcomes:

CO1	Learner will have knowledge of operation of switched capacitor circuits.
CO2	Learner will be able to design a filter network.
CO3	Learner will learn Data Converter Fundamentals.
CO4	Learner will be able to learn topology of PLL network.

UNIT I

Switched Capacitor filters: Introduction to Analog and Discrete Time signal processing, sampling theory, Nyqist and over sampling rates, Analog filters, analog amplifiers, lock in amplifiers,

UNIT II

Analog integrated and discrete time switched capacitor filters, non-idealities in switched capacitor filters, architectures for switched capacitor filters and their applications and design. Switched capacitor amplifiers.

UNIT III

Data converters: Basics of data converters, Types of data converters, types of ADCs, Successive approximation, dual slope, Flash type, pipelined ADCs, hybrid ADCs, high resolution ADCs, parallel path ADCs like time-interleaved and multi-channel converters.

UNIT IV

Types of DACs and their architectures, binary weighted DACs. Performance metrics of data converters, SNR, SFDR, SNDR.

UNIT V

Background and foreground techniques to improve performance of data converters, Green data converters (low power design).

UNIT VI

Frequency synthesizers and synchronization: Analog PLLs, Digital PLLs design and architectures, Delay locked loops design and architectures. Direct Digital Synthesis.

Textbooks / References:

1. R. Jacob Baker, CMOS mixed-signal circuit design, Wiley India, IEEE press, reprint 2008
2. R. Jacob Baker, Switched-Current Signal Processing and A/D Conversion Circuits: Design and Implementation, Wiley India IEEE press 2008.
3. Andrzej Handkiewicz, Mixed Signal Systems: a guide to CMOS circuit design, IEEE computer Society Press.
4. Walt Kester, Mixed Signal and DSP Design techniques, Engineering Analog Devices Inc, Engineering Analog Devices Inc, Publisher Newnes.
5. Bar-Giora Goldberg, Digital Frequency Synthesis Demystified, Published by Elsevier.

ELECTIVE IV
ANALYSIS AND DESIGN OF DIGITAL SYSTEMS USING VHDL

Weekly Teaching Hours   TH : 03   Tut: --

Scheme of Marking   TH :60   Tests : 20   IA: 20   Total : 100

Course Objective:

A	To prepare the student to understand the VHDL language feature to realize the complex digital systems.
B	To design and simulate sequential and concurrent techniques in VHDL
C	To explain modeling of digital systems using VHDL and design methodology
D	To explain predefined attributes and configurations of VHDL.
E	To Understand behavioral, non-synthesizable VHDL and its role in modern design

Course Outcomes:

CO1:	Learner will be able to model, simulate, verify, and synthesize with hardware description languages.
CO2:	Learner will be able to understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements
CO3:	Learner will be able to design digital logic circuits in different types of modeling
CO4:	Learner will be able to demonstrate timing and resource usage associated with modeling approach.
CO5:	Learner will be able to use computer-aided design tools for design of complex digital logic circuits.

UNIT I

An overview of design procedures for system design using CAD tools. Design verification tools.

UNIT II

Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

UNIT III

Characterizing hardware languages, objects and classes, signal assignments, concurrent and

sequential assignments. Structural specification of hardware.

UNIT IV

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

UNIT V

Data flow and behavioral description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioral description of hardware.

UNIT VI

CPU modeling for discrete design- Parwan CPU, behavioral description, bussing structure, data flow, test bench, a more realistic Parwan. Interface design and modeling. VHDL as a modeling language.

Textbooks / References:

1. Z.Navabi, VHDL Analysis and Modeling of Digital Systems, (2/e), McGraw Hill, 1998. 2. Perry, "VHDL (3/e)", McGraw Hill.2002
2. A. Dewey, Analysis and Design of Digital Systems with VHDL, CL-Engineering, 1996.
3. Z.Navabi, VHDL: modular design and synthesis of cores and systems, McGraw, 2007.
4. C. H. Roth, Jr., L.K.John, Digital Systems Design Using VHDL - Thomson Learning EMEA, Limited, 2008.
5. Recent literature in Analysis and Design of Digital Systems using VHDL.

INTERNET OF THINGS

Weekly Teaching Hours	TH : 03	Tut: --			
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100	

Course Objectives:

A	Students will be explored to the interconnection and integration of the physical world and the cyber space.
B	To provide ability to design and develop IOT devices.

Course Outcomes:

CO1	Learner will be able to understand the meaning of internet in general and IOT in terms of layers, protocols, packets peer to peer communication
CO2	Learner will be able to interpret IOT working at transport layer with the help of various protocols
CO3	Learner will be able to understand IOT concept at data link layer
CO4	Learner will be able to apply the concept of mobile networking to the internet connected devices
CO5	Learner will be able to measure and schedule the performance of networked devices in IOT
CO6	Learner will be able to analyze the challenges involve in developing IOT architecture

UNIT I

Introduction: What is the Internet of Things: History of IoT, about objects/things in the IoT, Overview and motivations, Examples of applications, IoT definitions, IoT Frame work, General observations, ITU-T views, working definitions, and basic nodal capabilities.

UNIT II

Fundamental IoT Mechanisms & Key Technologies : Identification of IoT objects and services, Structural aspects of the IoT, Environment characteristics, Traffic characteristics ,scalability, Interoperability, Security and Privacy, Open architecture, Key IoT Technologies ,Device Intelligence, Communication capabilities, Mobility support, Device Power, Sensor Technology, RFID technology, Satellite Technology.

UNIT III

Radio Frequency Identification Technology: Introduction, Principles of RFID, Components of an RFID system, Reader, RFID tags, RFID middleware, Issue. Wireless Sensor Networks: History and context, node, connecting nodes, networking nodes, securing communication.

UNIT IV

Wireless Technologies For IoT : Layer ½ Connectivity : WPAN Technologies for IoT/M2M, Zigbee /IEEE 802.15.4, Radio Frequency for consumer Electronics (RF4CE), Bluetooth and its low-energy profile , IEEE 802.15.6 WBANS, IEEE 802.15 WPAN TG4j, MBANS, NFC, dedicated short range communication(DSRC) & related protocols. Comparison of WPAN technologies cellular & mobile network technologies for IoT/M2M.

UNIT V

Governance of The Internet of Things: Introduction, Notion of governance, aspects of governance, Aspects of governance Bodies subject to governing principles, private organizations, International regulation and supervisor, substantive principles for IoT governance, Legitimacy and inclusion of stakeholders, transparency, accountability. IoT infrastructure governance, robustness, availability, reliability, interoperability, access. Future governance issues, practical implications, legal implications.

UNIT VI

Internet of Things Application Examples: Smart Metering, advanced metering infrastructure, e-Health/Body area network, City automation, automotive applications. Home automation, smart cards, Tracking, Over-The-Air passive surveillance/Ring of steel, Control application examples.

Textbooks / References:

1. Hakima Chaouchi, The Internet of Things, Connecting Objects to the Web, Wiley Publications
2. Daniel Minoli,Building the Internet of Things with IPv6 and MIPv6 The Evolving World of M2M Communications, Wiley Publications
3. Bernd Scholz-Reiter, Florian Michahelles, Architecting the Internet of Things, ISBN 978- 3842-19156-5, Springer.
4. Olivier Hersent, David Boswarthick, Omar Elloumi, The Internet of Things Key Applications and Protocols, ISBN 978-1-119-99435-0, Wiley Publications.

LINEAR ALGEBRA

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of fundamental concepts of linear algebra
B	To understand the importance of linear algebra and learn its applicability to practical problems

Course Outcomes:

CO1	Learner will learn to solve and analyze linear system of equation
CO2	Learner will analyze the direct notations, duality, adjointness, bases, dual bases in linear algebra
CO3	Learner will understand the concept of Linear transformations and matrices, equivalence, similarity.
CO4	Learner will be able to find eigen values and eigen vectors using characteristics polynomials
CO5	Learner will learn to find the singular value decomposition of the matrix
CO6	Learner will be to find the inverse of matrix

UNIT I

Fields Fq, R, C. Vector Spaces over a field, Fn, F[ɵ]=Polynomials in one Variable.

UNIT II

Direct Notations, Ket, bra vector, duality, adjointness, linear transformations, bases, dual bases.

UNIT III

Linear transformations and matrices, equivalence, similarity.

UNIT IV

Eigenvalues, eigenvectors, diagonalization, Jordoncanonical form

UNIT V

Bilinear and sesquilinear forms, inner product, orthonormal, bases, orthogonal decomposition, projections

UNIT VI

System of equations, generalized inverses.

Textbooks / References:

1. Ronald Shaw, Linear Algebra and Group Representations, AcademicPress, Volume I-1982.

2. Ronald Shaw, Linear Algebra and Group Representations, AcademicPress, Volume II-1983.

3. A. R. Rao, Bhima Sankaran, Linear Algebra, TRIM, 2nd Edition, Hindustan

NEURAL NETWORKS IN EMBEDDED APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To be able to use analogy of human neural network for understanding of artificial learning algorithms.
B	To give in-depth understanding of fundamental concepts of neural network
C	To exhibit the knowledge of radial basis function network

Course Outcomes:

CO1	Learner will be able to understand concept of fuzzy logic.
CO2	Learner will be able to understand embedded digital signal processor, Embedded system design and development cycle, applications in digital camera
CO3	Learner will be able to understand embedded systems, characteristics, features and applications of an embedded system
CO4	Learner will be able to design and utilization of fuzzy logic controller for various industrial applications
CO5	Learner will be able to implement of radial basis function, neural network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

UNIT I

Introduction to artificial neural networks, Fundamental models of artificial neural network, Perceptron networks, Feed forward networks, Feedback networks, Radial basis function networks, Associative memory networks

UNIT II

Self organizing feature map, Learning Vector Quantization, Adaptive resonance theory, Probabilistic neural networks, neocgnitron, Boltzmann Machine.

UNIT III

Optical neural networks, Simulated annealing, Support vector machines, Applications of neural network in Image processing,

UNIT IV

Introduction to Embedded systems, Characteristics, Features and Applications of an embedded system

UNIT V

Introduction to embedded digital signal processor, Embedded system design and development cycle, ANN application in digital camera,

UNIT VI

Implementation of Radial Basis Function, Neural Network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

Textbooks / References:

1. S N Sivanandam, S Sumathi, S N Deepa, "Introduction to Neural Networks Using Matlab 6.0", Tata McGraw Hill Publication
2. Simon Haykin, "Neural Networks: Comprehensive foundation", Prentice Hall Publication
3. Frank Vahid, TonyGivargis, "Embedded System Design A unified Hardware/ Software Introduction", Wiley India Pvt. Ltd.
4. Rajkamal, "Embedded Systems Architecture, Programming and Design," Tata McGraw-Hill

ELECTIVE V
RESEARCH METHODOLOGY

Weekly Teaching Hours	TH: 03	Tut: --		
Scheme of Marking	TH: 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To develop a research orientation among the scholars and to acquaint them with fundamentals of research methods.
B	To develop understanding of the basic framework of research process.
C	To identify various sources of information for literature review and data collection.
D	To understand the components of scholarly writing and evaluate its quality.

Course Outcomes::

CO1	Learner will learn the meaning, objective , motivation and type of research
CO2	Learner will be able to formulate their research work with the help of literature review
CO3	Learner will be able to develop an understanding of various research design and techniques
CO4	Learner will have an overview knowledge of modeling and simulation of research work
CO5	Learner will be able to collect the statistical data with different methods related to research work
CO6	Learner will be able to write their own research work with ethics and non-plagiarized way

UNIT I

Introduction: Defining research, Motivation and Course Objectives:, Types of research

Meaning of Research, Course Objectives: of Research, Motivation in Research, Types of Research

UNIT II

Research Formulation: Formulating The research Problem, Literature Review, Development of Working Hypothesis

UNIT III

Research Design: Important Concept in Research Design, Research Life Cycle, Developing Research Plan

UNIT IV

Overview of Modeling and Simulation: Classification of models, Development of Models, Experimentation, Simulation.

UNIT V

Statistical Aspects: Methods of Data Collection, Sampling Methods, Statistical analysis, Hypothesis testing.

UNIT VI

Research Report: Research Ethics, Plagiarism, Research Proposal, Report Writing and Writing Research Papers.

Textbooks / References:

1. J.P. Holman., Experimental Methods for Engineers
2. C.R. Kothari, Research Methodology, Methods & Techniques

WAVELET TRANSFORMS AND ITS APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of fundamental concepts of Wavelets.
B	To study wavelet related constructions, its applications in signal processing, communication and sensing.

Course Outcomes:

CO1	Learner will be able to understand the meaning of wavelet transform
CO2	Learner will understand the terminologies used in Wavelet transform with its properties
CO3	Learner will be able to model various filter bank using wavelet transformation
CO4	Learner will understand bases , orthogonal bases in wavelet transform
CO5	Learner will learn different types of wavelet transform
CO6	Learner will be able to design practical system using wavelet transform

UNIT I

Continuous Wavelet Transform Introduction, Continuous-time wavelets, Definition of the CWT, the VWT as a Correlation, Constant-Factor Filtering Interpretation and Time-Frequency Resolution, the VWT as an Operator, Inverse CWT, Problems.

UNIT II

Introduction to Discrete Wavelet Transform And Orthogonal Wavelet Decomposition: Introduction, Approximation of Vectors in Nested Linear Vector Subspaces, Examples of an MRA, Problems.

UNIT III

MRA, Orthonormal Wavelets, And Their Relationship To Filter Banks: Introduction, Formal Definition of an MRA, Construction of General Orthonormal MRA, a wavelet Basic for the MRA,

UNIT IV

Digital Filtering Interpretation, Examples of Orthogonal Basic Generating Wavelets, Interpreting Orthonormal MRAs for Discrete-Time signals, Miscellaneous Issues Related to PRQME Filter Banks, generating Scaling Functions and wavelets from Filter Coefficient, Problems.

UNIT V

Wavelet Transform And Data Compression: Introduction, Transform Coding, DTWT for Image Compression, Audio Compression, And Video Coding Using Multiresolution Techniques: a Brief Introduction.

UNIT VI

Other Application 0f Wavelet Transforms: Introduction, Wavelet denoising speckles Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transform of Projections, Communication application.

Textbooks / References:

1. C. Sidney Burrus, R. A. Gopianath, Pretice Hall, Introduction to Wavelet and Wavelet Transform
2. P.P.Vaidyanathan , PTR Prentice Hall, Englewood Cliffs , New Jersey, Multirate System and Filter Banks
3. N.J.Fliege , John Wiley & Sons, Multirate Digital Signal Processing
4. Raghuveer Rao, Ajit Bopardikar, Pearson Education Asia,Wavelet Transforms Introduction to Theory and Application
5. James S. Walker, "A Primer on Wavelets and their Scientific Applications", CRC Press, (1999).
6. Rao, "Wavelet Transforms", Pearson Education, Asia.

SEMINAR I

Weekly Teaching Hours	TH: -	Practical: 04	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The seminar shall be on the state of the art in the area of the wireless communication and computing and of student's choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

MINI PROJECT

Weekly Teaching Hours	TH: -	Practical: 04	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The mini project shall be based on the recent trends in the industry, research and open problems from the industry and society. This may include mathematical analysis, modelling, simulation, and hardware implementation of the problem identified. The mini project shall be of the student's choice and approved by the guide. The student has to submit the report of the work carried out in the prescribed format signed by the guide and head of the department/institute.

PROJECT MANAGEMENT AND INTELLECTUAL PROPERTY RIGHTS

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The Student has to choose this course either from NPTEL/MOOCs/SWAYAM pool. It is mandatory to get the certification of the prescribed course.

PROJECT-I

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

Project-I is an integral part of the final project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation that may include mathematical model/SRS/UML/ERD/block diagram/ PERT chart, and layout and design of the proposed system/work. As a part of the progress report of project-I work, the candidate shall deliver a presentation on progress of the work on the selected dissertation topic.

It is desired to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall submit the duly certified progress report of project -I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.

PROJECT-II

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 100	PR/OR: 100	Total: 200

In Project - II, the student shall complete the remaining part of the project which will consist of the simulation/ analysis/ synthesis/ implementation / fabrication of the proposed project work, work station, conducting experiments and taking results, analysis and validation of results and drawing conclusions.

It is mandatory to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.