Dr. Babasaheb Ambedkar Technological University

Course Structure and Syllabus

For

M. Tech. (Embedded Engineering)

Two Year (Four Semester) Course

(w.e.f. July 2017)

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,

Lonere-402103, Raigad (MS)

M. Tech. (Embedded Engineering)

Objectives

I. To serve the society and nation, by providing high quality engineering educational programs to the students, engaging in research and innovations that will enhance the skill and knowledge and assisting the economic development of the region, state, and nation through technology transfer.

II. To equip the postgraduate students with the state of the art education through research and collaborative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.

III. To encourage the post-graduates students, to acquire the academic excellence and skills necessary to work as Electronics and Telecommunication professional in a modern, ever-evolving world.

IV. To provide the broad understanding of social, ethical and professional issues of contemporary engineering practice and related technologies, as well as professional, ethical, and societal responsibilities.

V. To inculcate the skills for perusing inventive concept to provide solutions to industrial, social or nation problem.

Outcomes

I. Students of this program will have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.

II. Postgraduate students will gain an ability to design and conduct experiments, as well as to analyze and interpret data/results.

III. Learners of this program will built an ability to design and develop a system, components, devices, or process to meet desired needs.

IV. Masters students of this program will have an ability to work on multi-disciplinary teams and also as an individual for solving issues related to Electronics and Telecommunication.

V. Learners of this program will have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

VI. Postgraduate students will have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.

VII. Postgraduate students will have an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.

VIII. Learners of this program will have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, and user friendliness to cater needs for innovative product development.

IX. Postgraduate students will have an ability to solve contemporary social and industrial problems by engaging in life-long learning.

Dr. Babasaheb Ambedkar Technological University

Teaching and Examination Scheme for

M.Tech. (Embedded Engineering) w.e.f. July 2017

Sr. No.	Course Code	Name of the course	Hours/Week			Credit	Examination scheme				
							Theory		IA	PR/OR	TOTAL
			L	P	T		TH	Test			
First Semester											
01	MTESC101	System Design using Embedded Processors	03	--	1	04	60	20	20	--	**100**
02	MTESC102	Embedded Programming	03	--	1	04	60	20	20	--	**100**
03	MTESC103	Advanced Digital System Design	03	--	1	04	60	20	20	--	**100**
04	MTESE114	Elective-I	03	--	--	03	60	20	20	--	**100**
05	MTESE125	Elective-II	03	--	--	03	60	20	20	--	**100**
06	MTESC106	Communication Skills	02	--	--	02	--	--	25	25	**50**
07	MTESL107	PG Lab-I*	--	03	--	02	--	--	25	25	**50**
		Total for Semester I	**17**	**03**	**03**	**22**	**300**	**100**	**150**	**50**	**600**
Second Semester											
01	MTESC201	Product Design and Quality Management	03	--	1	04	60	20	20	--	**100**
02	MTESC202	Embedded OS and RTOS	03	--	1	04	60	20	20	--	**100**
03	MTESE233	Elective-III	03	--	--	03	60	20	20	--	**100**
04	MTESE244	Elective- IV	03	--	--	03	60	20	20	--	**100**
05	MTESE255	Elective-V- (Open to all)	03	--	--	03	60	20	20	--	**100**
06	MTESS206	Seminar-I	--	04	--	02	--	--	50	50	**100**
07	MTESP207	Mini-Project	--	04	--	02	--	--	50	50	**100**
		Total for Semester II	**15**	**8**	**02**	**21**	**300**	**100**	**200**	**100**	**700**
Third Semester											
1	MTESC301	Project Management & Intellectual Property Rights (Self Study)#	--	--	--	02	--	--	50	50	**100**
2	MTESP302	Project-I	--	--	--	10	--	--	50	50	**100**
		Total for Semester III	**--**	**--**	**-**	**12**	**--**	**--**	**100**	**100**	**200**
Fourth Semester											
1	MTESP401	Project-II	--	--	--	20	--	--	100	100	**200**
		Total for Semester IV	**--**	**--**	**--**	**20**	**--**	**--**	**100**	**100**	**200**
GRAND TOTAL											**1700**

* PG Lab-I –Practical shall be based on courses of first semester.

Student has to choose this course either from NPTEL/MOOC pool and submission of course completion certificate is mandatory.

Elective-I

A. Artificial Neural Networks and Applications
B. Digital VLSI design
C. Advanced Processors and its applications
D. Fault Tolerant Systems
E. Electromagnetic Interference and Compatibility

Elective-II

A. Design and Analysis of Algorithms
B. System On-Chip
C. Optical Fiber Communication
D. Statistical Signal Processing
E. Microelectronics

Elective-III

A. FPGA System Design
B. Wireless Sensor Network Design
C. VLSI and Microsystems
D. Information Security

Elective-IV

A. ASIC & SOC
B. Reconfigurable Computing
C. Electronic Packaging
D. Robotics and Machine Vision

Elective-V (Open)

A. Internet of Things
B. Linear Algebra
C. Neural Networks in Embedded Applications
D. Research Methodology
E. Wavelet Transforms and its Applications

SYSTEM DESIGN USING EMBEDDED PROCESSORS

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To impart the concepts and architecture of Embedded systems and to make the students capable of designing Embedded systems

Course Outcomes:

CO1	Learner will understand the Concepts and Architecture of Embedded Systems
CO2	Learner will get knowledge of ARM processor
CO3	Learner will be able to describe Cortex-M3 processor
CO4	Learner will be able to compile program with Cortex M3 processor
CO5	Learner will be able to distinguish between different peripherals and debugging tools

UNIT I

Embedded Concepts Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, and Software architecture, Application Software, Communication Software, Development and debugging Tools.

UNIT II

ARM Architecture Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.

UNIT III

Overview of Cortex-M3 Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.

UNIT IV

Cortex-M3 Implementation Overview: Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus. Exceptions: Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call. NVIC: Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer. Interrupt Behavior: Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency

UNIT V

Cortex-M3/M4 Programming: Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. Exception Programming: Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. Memory Protection UNIT and other Cortex-M3 features: MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication.

UNIT VI

Cortex-M3/M4 Microcontroller STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control. STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART. Development & Debugging Tools: Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.

Textbooks / References:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.

2. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", 2006, Elsevier.

1. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education

2. Cortex-M series-ARM Reference Manual

3. Cortex-M3 Technical Reference Manual (TRM)

4. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.

5. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers

6. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual

7. ARM Company Ltd. "ARM Architecture Reference Manual– ARM DDI 0100E"

8. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).

9. Ajay Deshmukh, "Microcontroller - Theory & Applications", Tata McGraw Hill

10. Arnold. S. Berger, "Embedded Systems Design - An introduction to Processes, Tools and Techniques", Easwer Press

11. Raj Kamal, "Microcontroller - Architecture Programming Interfacing and System Design" 1st Edition, Pearson Education

12. P.S Manoharan, P.S. Kannan, "Microcontroller based System Design", 1st Edition, Scitech Publications

EMBEDDED PROGRAMMING

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	This subject is framed to set the required background in embedded system concepts, Fundamentals of Linux OS and 'C' language for the rest of the modules.
B	It aims at familiarizing the students in embedded concepts and programming in 'C'.
C	This module covers the advanced topics in 'C' such as Memory management,
D	Pointers, Data structures which are of high relevance in embedded software is considered in depth.
E	The syllabus also covers the topic 'scripting languages for embedded systems'

Course Outcomes:

CO1	Learner will be able to develop advanced programs in Embedded C
CO2	Learner will be able to get knowledge in Embedded OS (Linux) fundamentals
CO3	Learner will be able to develop programs using scripting languages
CO4	Learner will be able to model and analyze real time embedded systems
CO5	Learner will be able to correlate relevance of programming languages in embedded systems
CO6	Learner will be able to compare scripting languages

UNIT I

Embedded OS Fundamentals (Linux) Introduction: Operating System Fundamentals, General Linux Architecture, Linux Kernel, Linux file systems, ROOTFS, Sysfs and Procfs,

UNIT II

Embedded Linux: Booting Process in Linux, boot loaders, U-boot, Kernel Images, Linux File systems. GNU Tools: gcc, gdb, gprof, Makefiles

UNIT III

Embedded C Programming Review of data types –scalar types-Primitive types-Enumerated types Subranges, Structure types-character strings –arrays- Functions Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly.

UNIT IV

Embedded programming issues - Reentrancy, Portability, Optimizing and testing embedded C programs. Modelling Language for Embedded Systems: Modeling and Analysis of RealTime and Embedded systems

UNIT V

Embedded Applications using Data structures Linear data structures– Stacks and Queues Implementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures – Trees and Graphs Object Oriented programming basics using C++ and its relevance in Embedded systems..

UNIT VI

Scripting Languages for Embedded Systems Shell scripting, Programming basics of Python, Comparison of scripting languages

Textbooks / References:

1. C Programming language, Kernighan, Brian W, Ritchie, Dennis M, Embedded C,Michael J. Pont, Addison Wesley
2. Jivan S. Parab, Vinod G. Shelake, Rajanish K.Kamot, and Gourish M.Naik, "Exploring C for Microcontrollers- A Hands on Approach", Springer.
3. Daniel W. Lewis, Fundamentals of embedded software where C and assembly meet, Pearson Education, 2002.
4. Bruce Powel Douglas, Real time UML, second edition: Developing efficient objects for embedded systems, 3rd Edition 1999, Pearson Education.
5. Steve Heath, Embedded system design, Elsevier, 2003.
6. David E. Simon, An Embedded Software Primer, Pearson Education, 2003.
7. Herbert Schildt, The Complete Reference C++, TMH
8. Bjarne Stoustrup,C++ programming language, Addison-Wesley
9. Tom Swan , GNU C++ For LinuxPrentice, Hall India
10. Robert Lafore , Object_Oriented programming in C++, Galgotia publications
11. Peter B. Galvin, Abraham Silberschatz, Gerg Gagne, Operating System Concepts, Wiley Publishers
12. Jones, M Tims GNU/LINUX Application Programming,

ADVANCED DIGITAL SYSTEM DESIGN

Weekly Teaching Hours	TH: 03	Tut: 01		
Scheme of Marking	TH: 60	Tests: 20	IA: 20	Total: 100

Course Objectives:

A	To prepare students for the design of practical digital hardware systems using VHDL.
B	To introduce students to the fundamentals of combination logic design and then to sequential circuits (both synchronous and asynchronous).
C	To provide opportunities to synthesize the designs (using both schematic capture and VHDL) for implementation in FPGAs.

Course Outcomes:

CO1	Learner will be able to differentiate combinational and sequential circuits
CO2	Learner will be able to design asynchronous sequential circuits
CO3	Learner will be able to express different aspects VHDL
CO4	Learner will be able to detect faults in logic circuits
CO5	Learner will be able to realize combinational circuits using HDL
CO6	Learner will get knowledge of FPGA

UNIT I

Introduction to Digital Design Combinational Circuit Design, Synchronous Sequential Circuit Design - Mealy and Moore model, State machine design, Analysis of Synchronous sequential circuit, State equivalence, State Assignment and Reduction, Analysis of Asynchronous Sequential Circuit, flow table reduction, races, state assignment

UNIT II

Design of Asynchronous Sequential Circuit, Designing with PLDs – Overview of PLDs – ROMs, EPROMs – PLA – PAL - Gate Arrays – CPLDs and FPGAs, Designing with ROMs - Programmable Logic Arrays - Programmable Array logic, PAL series 16 & 22 – PAL22V10 - Design examples.

UNIT III

VHDL Basics – Introduction to HDL – Behavioral modeling – Data flow modeling – Structural modeling – Basic language elements – Entity – Architecture – Configurations – Subprograms & operator overloading – Packages and libraries – Test Bench – Advanced Features – Model simulation

UNIT IV

Realization of combinational and sequential circuits using HDL – Registers – Flip flops – counters – Shift registers –Multiplexers – sequential machine – Multiplier – Divider, Introduction to Synthesis and Synthesis Issues.

UNIT V

Testing, Fault Modelling And Test Generation – Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Test generation for combinational logic circuits – Testable combinational logic circuit design, Introduction to Design for Testability, BST

UNIT VI

FPGA - FPGAs - Logic blocks, Routing architecture, Design flow technology - mapping for FPGAs, Xilinx FPGA Architecture, Xilinx XC4000 - ALTERA's FLEX 8000, Design flow for FPGA Design, Case studies: Virtex II Pro.

Textbooks / References:

1. Parag K. Lala, "Digital System Design using programmable Logic Devices", Prentice Hall, NJ, 1994
2. Geoff Bestock, "FPGAs and programmable LSI; A Designers Handbook", Butterworth Heinemann, 1996
3. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", John Wiley & Sons Inc.
4. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications, 2002
5. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992
6. Jesse H. Jenkins, "Designing with FPGAs and CPLDs", Prentice Hall, NJ,1994
7. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
8. Kevin Skahill, "VHDL for Programmable Logic", Addison -Wesley, 1996
9. Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGRAW-Hill, 1998
10. Digital Circuits and Logic Design – Samuel C. Lee , PHI
11. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
12. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2000

ELECTIVE-I

ARTIFICIAL NEURAL NETWORKS AND APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course objectives:

A	To provide in-depth understanding of fundamental theory and concepts of computational intelligence methods
B	To understand the fundamental theory and concepts of neural networks, neuro-modeling, several neural network paradigms and its applications.

Course Outcomes:

CO1	Learner will be able to articulate analogy of human neural network for understanding of artificial learning algorithms.
CO2	Learner will be able to analyze radial basis function network.
CO3	Learner will be able to analyze neural network architecture & basic learning algorithms.
CO4	Learner will be able to understand mathematical modeling of neurons, neural networks.
CO5	Learner will be able to analyze training, verification and validation of neural network models
CO6	Learner will be able to design Engineering applications that can learn using neural networks

UNIT I

Brain Style Computing: Origins and Issues**,** Biological neural networks, Neuron Abstraction, Neuron Signal.

UNIT II

Functions, Mathematical Preliminaries, Artificial Neurons, Neural Networks and Architectures Pattern analysis tasks: Classification, Clustering, mathematical models of neurons, Structures of neural networks, learning principles.

UNIT III

Feed forward neural networks: Pattern classification using perceptron, Multilayer feed forward neural networks (MLFFNNs), Pattern classification and regression using MLFFNNs, Error back-propagation learning, Fast learning methods: Conjugate gradient method.

UNIT IV

Auto-associative neural networks, Pattern storage and retrieval, Hopfield model, recurrent neural networks, Bayesian neural networks,

UNIT V

Radial basis function networks: Regularization theory, RBF networks for function approximation, RBF networks for pattern classification

UNIT VI

Self-organizing maps: Pattern clustering, Topological mapping, Kohonen's self-organizing map Introduction to cellular neural network, Fuzzy neural networks, and Pulsed neuron models recent trends in Neural Networks

Textbooks / References:

1. Satish Kumar, Neural Networks, A Classroom Approach, Tata McGraw-Hill, 2003
2. JacekZurada, Introduction to Artificial Neural Networks, Jaico Publishing House, 1997.
3. S.Haykin, Neural Networks, A Comprehensive Foundation, Prentice Hall, 1998.
4. C.M.Bishop, Pattern Recognition and Machine Learning, Springer, 2006.
5. B.Yegnanarayana, Artificial Neural Networks, Prentice Hall of India, 1999.
6. L.O. Chua and T. Roska, Cellular Neural Networks and Visual Computing Foundation and Applications, Cambridge Press, 2002.

ELECTIVE-I

DIGITAL VLSI DESIGN

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To create models of moderately sized CMOS circuits that realize specified digital functions
B	Have an understanding of the characteristics of CMOS circuit construction
C	To complete a significant VLSI design project having a set of objective criteria and design constraints.

Course Outcomes:

CO1	Learner will be aware about the trends in semiconductor technology, and how it impacts scaling and performance.
CO2	Learner will be able to model moore and melay machine
CO3	Learner will be able to classify complex programmable logic devices
CO4	Learner will be able to extend his knowledge to CMOS subsystem design
CO5	Learner will be able to paraphrase floor planning concept

UNIT I

Introduction to VLSI Circuits

Introduction to MOSFETs**:** MOS Transistor Theory –Device Structure and Physical Operation, Current Voltage Characteristics, Fabrication, MOS Capacitor, Body Effect, Temperature Effects, Channel Length Modulation, Latch-up. MOS Inverter: MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Transistor Sizing, Voltage Transfer Characteristics, Power Dissipation, Noise Margin, Power Delay Product, Energy dissipation. MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters. Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates: Primitive Logic Gates

UNIT II

Digital Circuit Design using VHDL

Design of sequential circuits, asynchronous and synchronous design issues, state machine modeling (Moore and mealy machines), packages, sub programs, attributes, test benches.

UNIT III

Programmable Logic Devices

Complex Programmable Logic Devices – Architecture of CPLD, Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT IV

CMOS Subsystem Design

Semiconductor memories, memory chip organization, Random Access Memories (RAM), Static RAM (SRAM), standard architecture, 6T cell, sense amplifier, address decoders, timings. Dynamic RAM (DRAM), different DRAM cells, refresh circuits, timings.

UNIT V

Floor Planning and Placement

Floor planning concepts, shape functions and floor plan sizing, Types of local routing problems, Area routing, channel routing, global routing, algorithms for global routing.

UNIT VI

Fault Tolerance and Testability

Types of fault, stuck open, short, stuck at 1, 0 faults, Fault coverage, Need of Design for Testability (DFT), Controllability, predictability, testability, built in Self Test (BIST), Partial and full scan check, Need of boundary scan check, JTAG, Test Access Port (TAP) controller

Textbooks / References:

1. Neil H. Weste and Kamran, Principles of CMOS VLSI Design, Pearson Publication
2. John F. Wakerly, Digital Design, Principles and Practices, Prentice Hall Publication
3. Douglas Perry, VHDL, McGraw Hill Publication.
4. Charles Roth, Digital System Design using VHDL, McGraw Hill Publication.
5. Data Sheets of PLDs.
6. Sung-Mo (Steve) Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata
7. McGraw Hill Publication.

ELECTIVE- I

ADVANCED PROCESSORS AND ITS APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course objectives:

A	Architect a microprocessor or microcontroller system and estimate the required hardware and software resources.
B	Select a microprocessor or microcontroller suitable to the application.
C	Perform the detailed hardware design of a microprocessor or microcontroller system.
D	Program the microprocessor or microcontroller using suitable techniques including use of allocation schemes and device drivers.
E	Find effective solutions to a wide range of real-world microprocessor and microcontroller applications.

Course Outcomes:

CO1	Learner will be able to express architecture of typical 8 bit microprocessor
CO2	Learner will be able to summarize various aspects of 16 bit microprocessor
CO3	Learner will be able to interface IO devices to microprocessor
CO4	Learner will be able to interface analog IO devices to microprocessor
CO5	Learner will be able to express 8 bit microcontroller and architecture

UNIT I

Review of basic microprocessor and microcomputer concepts and the architecture and instruction set of a typical 8 bit microprocessor.

UNIT II

ADVANCED PROCESSORS: - Overview of 16-bit/32-bit/64 bit Intel based microprocessors. Arithmetic and I/O co-processor architecture. Register details, operation-addressing modes & instruction set of a typical 16-bit microprocessor, assembly language programming for the processor introduction to multiprocessing.

UNIT III

PROGRAMMIABLE SUPPORT CHIPS:- Programmable parallel interface chip (e.g. 8255) functional schematic. Pin function operating mode interface with microprocessor chip programming serial communication interface chip (e.g. 8251) functional schematic pin function.

UNIT IV

Operating mode interface with processor mode and command words for the chip programmable interrupt controller (8259) functional schematic pin function single and cascaded operation interface with microprocessor and I/O devices Programmable interval timer (8253) functional schematic pin functions. Modes of operations.

UNIT V

ANALOG INPUT AND OUTPUT: - Microprocessor compatible ADC & DAC chips interfacing ADC with multiplexer with ADC, microprocessor use of sample and hold circuit interfacing DAC with microprocessor.

UNIT VI

MICROCONTROLLER:- Hardware and software integration in microprocessor control system. An overview of 8-bit microcontroller architecture and instruction set.

Textbooks / References:

1. Advanced Microprocessor A.K.Ray, K.M.Bhurchandi TMH

2. Microprocessor Gaonkar

3. Microprocessor, Hardware & Programming Douglas V Hall

ELECTIVE-I

FAULT TOLERANT SYSTEMS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of the fundamental concepts of fault-tolerance.
B	To develop skills in modeling and evaluating fault-tolerant architectures in terms of reliability, availability and safety
C	To gain knowledge in sources of faults and means for their prevention and forecasting

Course Outcomes:

CO1	Learner will be able to analyze the risk of computer failures and their peculiarities compared with other equipment failures.
CO2	Learner will be able to analyze advantages and limits of fault avoidance and fault tolerance techniques.
CO3	Learner will be able to distinguish threat from software defects and human operator error as well as from hardware failures.
CO4	Learner will be able to analyze different forms of redundancy and their applicability to different classes of dependability requirements.
CO5	Learner will be able to choose among commercial platforms (fault-tolerant or non fault-tolerant) on the basis of dependability requirements.
CO6	Learner will be able to demonstrate the use of fault tolerance in the design of application software.
CO7	Learner will be able to analyze relevant factors in evaluating alternative system designs for a specific set of requirements.
CO8	Learner will be aware of the subtle failure modes of "fault-tolerant" distributed systems, and the existing techniques for guarding against them.
CO9	Learner will be able to analyze cost-dependability trade-offs and the limits of computer system dependability.

UNIT I

Modelling and Logic Simulation:

Functional modelling at the logic and the register level, Structural models, Level of modelling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation, different delay models, Hazard Detection.

UNIT II

Fault Modelling and Fault Simulation:

Logical fault models, Fault detection and Redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, Multiple stuck fault model, stuck RTL variables, Fault variables. Testing for single stuck fault and Bridging fault, General fault simulation techniques, Serial and Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis.

UNIT III

Compression techniques and self-checking System:

General aspects of compression techniques, ones-count compression, transition –count compression, Parity –check compression, Syndrome testing and Signature Analysis,

UNIT IV

Self-checking Design, Multiple –Bit Errors, self–checking checkers, Parity –check function , totally self-checking m/n code checkers, totally self-checking equality checkers, Self-checking Berger code checkers and self-checking combinational circuits.

UNIT V

Testability: Testability, trade-offs, Ad hoc Design for Testability techniques, Introduction to BIST concept, Test pattern generation for BIST

UNIT VI

Self-testing circuits for systems, memory & processor testing, PLA-testing, automatic test pattern generation and Boundary Scan Testing JTAG.

Textbooks / References:

1. M.Abramovici, M.A. Breuer, A.D. Friedman, “Digital systems testing and testable design”,Jaico Publishing House.
2. Kwang-Ting (Tim) Cheng and Vishwani D. Agrawal, “Unified Methods for VLSI Simulation and Test Generation”The Springer International Series in Engineering(Jun 30, 1989).

ELECTIVE-I

ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To familiarize with the fundamentals that are essential for electronics industry in the field of EMI / EMC
B	To understand EMI sources and its measurements.
C	To understand the various techniques for electromagnetic compatibility.

Course Outcomes:

CO1	Learner will acquire knowledge of EMI / EMC sources and their standards
CO2	Lerner will be able to measure different parameters of interference in EM
CO3	Learner will be able to reduce the interference within EM devices
CO4	Lerner will be able to illustrate the physical and statistical model of EM devices
CO5	Lerner will be able to analyze the EM devices in terms of Computer Based Modeling and Simulation
CO6	Learner will be able to design electronic systems that function without errors or problems related to electromagnetic compatibility.

UNIT I

Introduction to EMI / EMC:

EMI / EMC Standards, Introduction to E, H, Near and far field radiators, Receptors and antennas, Different types of EMI sources and possible remedies.

UNIT II

Measurement techniques in EMI: Open area test sites, Radiated interference measurements, Conducted interference measurements, Interference immunity.

UNIT III

EMI reduction techniques: Grounding, Shielding, Bonding, EMI filters.

UNIT IV

Probabilistic and Statistical Physical Model: Introduction, Probability considerations,

Statistical Physical Models of EMI / EMC, EMC of terrestrial radio communication systems.

UNIT V

Computer Based Modeling and Simulation: Computer Based Modeling and Simulation of EMI Models and Signal Integrity.

UNIT VI

Electrostatic Discharge (ESD): Introduction, Accumulation of Static Charge on Bodies Charging and Charge Separation, Human Body as Source of ESD, ESD Waveforms, Human Body Circuit Model, ESD Generator and ESD Test

Textbooks / References:

1. Engineering Electromagnetic Compatibility, Principles and Measurement Technologies; V. Prasad Kodali; IEEE Press
2. Electromagnetic Compatibility, Principles and Applications; Devid A. Weston, Marcol Dekker, Inc New York.
3. Dipak L. Sengupta, Valdis V. Liepa, Applied Electromagnetics And Electromagnetic C0mpatibility, A John Wiley & Sons, Inc. Publication

ELECTIVE-II

DESIGN AND ANALYSIS OF ALGORITHMS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	The student should be made to: Learn the algorithm analysis techniques.
B	Become familiar with the different techniques.
C	Understand the limitations of Algorithm power.

Course Outcomes:

CO1	Learner will be able to Design algorithms for various computing problems.
CO2	Learner will be able to Analyze the time and space complexity of algorithms.
CO3	Learner will be able to Critically analyze the different algorithm design techniques for a given problem.
CO4	Learner will be able to Modify existing algorithms to improve efficiency.

UNIT I

Introduction

Notion of an Algorithm – Fundamentals of Algorithmic Problem Solving – Important Problem types – Fundamentals of the Analysis of Algorithm Efficiency – Analysis Framework – symptotic Notations and its properties – Mathematical analysis for Recursive and Non-recursive algorithms.

UNIT II

Brute Force And Divide-And-Conquer

Brute Force - Closest-Pair and Convex-Hull Problems-Exhaustive Search – Traveling Salesman Problem - Knapsack Problem - Assignment problem. Divide and conquer methodology – erge sort – Quick sort – Binary search – Multiplication of Large Integers – Strassen's Matrix MultiplicationClosest-Pair and Convex-Hull Problems.

UNIT III

Dynamic Programming And Greedy Technique

Computing a Binomial Coefficient – Warshall's and Floyd' algorithm – Optimal Binary Search Trees – Knapsack Problem and Memory functions. Greedy Technique– Prim's algorithm- Kruskal's Algorithm - Dijkstra's Algorithm-Huffman Trees.

UNIT IV

Iterative Improvement

The Simplex Method-The Maximum-Flow Problem – Maximm Matching in Bipartite Graphs- the Stable marriage Problem.

UNIT V

Coping With The Limitations Of Algorithm Power

Limitations of Algorithm Power-Lower-Bound Arguments-Decision Trees-P, NP and NP-Complete Problems--Coping with the Limitations - Backtracking – n-Queens problem –

UNIT VI

Hamiltonian Circuit Problem – Subset Sum Problem-Branch and Bound – Assignment problem – Knapsack Problem – Traveling Salesman Problem- Approximation Algorithms for NP – Hard Problems – Traveling Salesman problem – Knapsack problem

Textbooks / References:

1. Anany Levitin, Introduction to the Design and Analysis of Algorithms, Third Edition, Pearson Education, 2012.
2. Thomas H.Cormen, Charles E.Leiserson, Ronald L. Rivest and Clifford Stein, Introduction to Algorithms, Third Edition, PHI Learning Private Limited, 2012.
3. Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman,Data Structures and Algorithms, Pearson Education, Reprint 2006.
4. Donald E. Knuth, The Art of Computer Programming, Volumes 1& 3 Pearson Education, 2009.
5. Steven S. Skiena, The Algorithm Design Manual, Second Edition, Springer, 2008.

ELECTIVE-II

SYSTEM ON CHIP

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide students with a sound knowledge of VLSI systems covering the following:
B	To provide an in-depth understanding of what SoC is and what are the differences between SoC and Embedded System
C	To provide an in-depth understanding of basics of System on Chip and Platform based design.
D	To provide an in-depth understanding of issues and tools related to SoC design and implementation.

Course Outcomes:

CO1	Learner will be able to interpret nature of hardware and software, its data flow modeling and implementation techniques.
CO2	Learner will be able to analyze the micro-programmed architecture of cores and processors.
CO3	Learner will be able to demonstrate system on chip design models.
CO4	Learner will be able to hypothesize and synthesize working of advanced embedded systems.
CO5	Learner will be able to develop design SOC controller.
CO6	Learner will be able to design, implement and test SOC model.

UNIT I

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD.

UNIT II

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code,

UNIT III

System on Chip, concept, design principles, portable multimedia system, SOC modelling, hardware/software interfaces, synchronization schemes, memory mapped Interfaces , coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model .

UNIT IV

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

UNIT V

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS

UNIT VI

SOC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

Textbooks / References:

1. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer
2. Sanjay Churiwala, SapanGarg , Principles of VLSI RTL Design A Practical Guide, Springer
3. Youn-Long Steve Lin, Essential Issues in SOC Design, Designing Complex Systems-on-Chip, Springer

ELECTIVE-II

OPTICAL FIBER COMMUNICATION

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To expose the students to the basics of signal propagation through optical fibers, fiber impairments, components and devices and system design.
B	To provide an in-depth understanding needed to perform fiber-optic communication system engineering calculations, identify system tradeoffs, and apply this knowledge to modern fiber optic systems.

Course Outcomes:

CO1	Learner will be able to recognize and classify the structures of Optical fiber and types.
CO2	Learner will be able to demonstrate electromagnetic and mathematical analysis of light wave propagation.
CO3	Learner will be able to analyze fabrication techniques of different optical fibers.
CO4	Learner will be able to interpret behavior of pulse signal and various loss mechanism.
CO5	Learner will be able to interpret Dispersion compensation mechanism, Scattering effects and modulation techniques.
CO6	Learner will be able to interpret working of Fiber based devices.

UNIT I

Introduction and importance of Fiber Optics Technology, Ray analysis of optical fiber: Propagation mechanism of rays in an optical fiber, Meridional rays, Skew rays, Fiber numerical aperture, dispersion.

UNIT II

Electromagnetic (modal) analysis of Step index multimode fibers: Wave equation and boundary conditions, Characteristics equation, TE, TH and Hybrid modes, Weakly guiding approximation, linearly polarized modes, Single mode fiber, V parameter, Power confinement and mode cutoff, Mode field diameter.

UNIT III

Graded-index fiber: Modal analysis of graded index fiber, WKB analysis, Optimum profile. Experimental techniques in fiber optics: Fiber fabrication (OVD, VAD, CVD, MCVD, PMCVD etc.) and characterization, Splices, Connectors and fiber cable.

UNIT IV

Loss mechanism in optical fiber: Absorption loss, scattering loss, bending loss, splice loss. Pulse propagation, Dispersion and chirping in single mode fibers: Pulse propagation in non-dispersive and dispersive medium, Pulse broadening and chirping, Group and phase velocity, Intermodal and intramural dispersion, Group velocity (material and waveguide) dispersion, Higher order dispersion, Fiber bandwidth.

UNIT V

Dispersion compensation mechanism: Dispersion tailored and dispersion compensating fibers, Fiber Birefringence and polarization mode dispersion, Fiber bandwidth, Nonlinear effects in optical fiber: Stimulated Raman Scattering, Stimulated Brillouin Scattering, Self-Phase, Modulation, Cross Phase Modulation, and Optical Solitons.

UNIT VI

Fiber based devices: Erbium-doped fiber amplifiers and lasers, Fiber Bragg gratings, Optical Fiber Sensors. Photonic Crystal fibers.

Textbooks / References:

1. K. Ghatak & K. Thyagarajan, Introduction to Fiber Optics, Cambridge University Press (1998).
2. P. Agarwal, Fiber Optic Communication Systems, John Wiley Sons (1997).
3. John A. Buck, Fundamentals of Optical Fibers, Wiley Interscience, (2004).
4. J. M. Senior, Optical Fiber Communication, Prentice Hall (1999).
5. Keiser, Optical Fiber Communications, McGraw Hill (2000).
6. K. Okamoto, Fundamentals of Optical Waveguides, Academic Press, (2000).
7. K. Iizuka, Elements of Photonics Vol I &II, Wiley-Interscience (2002).
8. W. Prather et.al, Photonic Crystal, Wiley (2009).

ELECTIVE-II

STATISTICAL SIGNAL PROCESSING

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of more advanced probability theory, leading into random process theory and focus on discrete time methods.
B	To provide in-depth understanding of fundamental concepts of statistical signal processing,

Course Outcomes:

CO1	Learner will be able to generalize the properties of statistical models in the analysis of Signals using Stochastic processes.
CO2	Learner will be able to compare different Stochastic Processes and Models.
CO3	Learner will be able to demonstrate optimum linear filter algorithms and structures.
CO4	Learner will be able to Differentiate the prominence of various spectral estimation techniques for Achieving higher resolution in the estimation of power spectral density.
CO5	Learner will be able to visualize Least Square Filtering and Computation techniques.
CO6	Learner will be able to interpret adaptive filtering and its applications.

UNIT I

Introduction

Random Signals, Spectral Estimation, Adaptive Filtering, Random Variables, Distribution and Density Functions, Random Vectors: Definition, Transformation and Linear Combination of Random Vectors Linear System with Stationary Input, Innovations and Representation of Real Vectors, DT Stochastic Process: Stationarity, Ergodicity and Frequency Domain Representation of SP, Principles of Estimation.

UNIT II

Stochastic Processes and Models

Characterization of DT Stochastic Process, Correlation Matrix, Properties of Correlation Matrix, Stochastic Models: MA and AR Models, ARMA Models Hold Decomposition, Asymptotic Stationarity of AR Process, Yule Walker Equations, Power Spectral Density, Properties of Power Spectral Density Transmission of Stationary Process Through a Linear Filter, Other Statistical Characteristics of Stochastic Process Power Spectral Estimation, Spectral Correlation Density, Polyspectra

UNIT III

Optimum Linear Filters

Optimum Signal Estimation, Linear Mean Square Estimation, Solution of Normal Equations, Optimum FIR Filters, Linear Prediction: Linear Signal Estimation, Forward Linear Estimation, Backward Linear Estimation, Stationary Processes and Properties, Optimum IIR Filters, Inverse Filtering and Deconvolution.

UNIT IV

Algorithms and Structures For Optimum Filters.

Fundamentals of Order-Recursive Algorithms, Interpretation of Algorithmic Quantities, Order-Recursive Algorithms for Optimum FIR Filters, Algorithms of Levinson and Levinson-Durbin, Lattice Structure for Optimum Filters, Schur Algorithm, Triangularization and Inverse of Toeplitz Matrices, Kalman Filter Algorithm.

UNIT V

Least Square Filtering

Principle of LS, Linear Least Square Error Estimation, Least Square Filter, Linear Least Square Signal Estimation, LS Computation using Normal Equations, LS Computation using Orthogonalization Techniques, LS Computation using Singular Value Decomposition Techniques, Problems.

UNIT VI

Adaptive Filtering

Introduction, Typical Applications, Principles of Adaptive Filters, Method of Steepest Decent, LMS Algorithm, RLS Adaptive Filter, Fast RLS Algorithms for FIR Filtering, Frequency Domain and Subband Adaptive Filters.

Textbooks / References:

1. Adaptive Filter Theory; S. Haykin; PHI.
2. Statistical and Adaptive Signal Processing; D. G. Manolakis, V. K. Ingle, S. M. Kogon; McGraw Hill.

ELECTIVE-II

MICROELCTRONICS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH : 60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding and to be able to apply basic concepts of semiconductor physics relevant to devices
B	To be able to analyze and design microelectronic circuits for linear amplifier and digital applications

Course Outcomes:

CO1	Learner will be able to discuss MOS structure in terms of different parameters
CO2	Learner will be able to express different CMOS technologies
CO3	Learner will get knowledge of design rules for the CMOS design
CO4	Learner will be able to understand how devices and integrated circuits are fabricated and describe discuss modern trends in the microelectronics industry
CO5	Learner will be able to determine the frequency range of simple electronic circuits and understand the high frequency limitations of BJTs and MOSFETs
CO6	Learner will be able to design simple devices and circuits to meet stated operating specifications

UNIT I

Ideal I-V Characteristics, C-V Characteristics: MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects: Velocity Saturation and Mobility Degradation, Channel Length Modulation, Body Effect, Sub threshold Conduction, Junction Leakage, Tunneling, Temperature and Geometry Dependence. DC Transfer characteristics: Complementary CMOS Inverter DC Characteristics, Beta Ratio Effects, Noise Margin, Ratio Inverter Transfer Function, Pass Transistor DC Characteristics, Tristate Inverter, Switch- Level RC Delay Models

UNIT II

CMOS Technologies: Background, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Isolation, Gate Oxide, Gate and Source/Drain Formation, Contacts and Metallization, Passivation, Metrology.

UNIT III

Layout Design Rules: Design Rules Background, Scribe Line and Other Structures, MOSIS Scalable CMOS Design Rules, Micron Design Rules. CMOS Process Enhancements:

Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Layout Design rules, Gate Layout, Stick Diagrams.

UNIT IV

Delay Estimation: RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, choosing the Best Number of Stages. Power Dissipation: Static Dissipation, Dynamic Dissipation, Low-Power Design. Interconnect: Resistance, Capacitance, Delay, Cross talk. Design Margin: Supply Voltage, Temperature, Process Variation, Design Corners. Reliability, Scaling.

UNIT V

Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip-Flops, Circuit Families: Static CMOS, Ratioed Circuits,

UNIT VI

Cascode Voltage Switch Logic, Dynamic Circuits, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Analog Circuit Designs, MOS Small-signal Models, Common Source Amplifier, The CMOS Inverter as an Amplifier, Current Mirrors, Differential Pairs, CMOS Operational Amplifier topologies, Digital to Analog Converters, switched capacitors, Analog to Digital Converters, RF Circuits

Textbooks / References:

1. J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Pearson/PHI (Low Price Edition)
2. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill
3. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill
4. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, Second Edition, Oxford University Press
5. P. Gray, P. J. Hurst, S. H. Lewis and R. Meyer, Analysis and Design of Analog Integrated Circuits, Fourth Edition,Wiley, 2001. (Low Price Edition)

COMMUNICATION SKILLS

Weekly Teaching Hours	TH: 02		Practical: -	
Scheme of Marking	TH: --	IA: 25	PR/OR: 25	Total: 50

Course Objectives:

A	To become more effective confident speakers and deliver persuasive presentations
B	To develop greater awareness and sensitivity to some important considerations in interpersonal communication and learn techniques to ensure smoother interpersonal relations

Course Outcomes:

CO1	Learner will be able to understand the fundamental principles of effective business communication
CO2	Learner will be able to apply the critical and creative thinking abilities necessary for effective communication in today's business world
CO3	Learner will be able to organize and express ideas in writing and speaking to produce messages suitably tailored for the topic, objective, audience, communication medium and context
CO4	Learner will be able to demonstrate clarity, precision, conciseness and coherence in your use of language
CO5	Learner will be able to become more effective confident speakers and deliver persuasive presentations

UNIT I

Introduction to communication, Necessity of communication skills, Features of good communication, Speaking skills, Feedback & questioning technique, Objectivity in argument

UNIT II

Verbal and Non-verbal Communication, Use and importance of non-verbal communication while using a language, Study of different pictorial expressions of non-verbal communication and their analysis

UNIT III

Academic writing, Different types of academic writing, Writing Assignments and Research Papers, Writing dissertations and project reports

UNIT IV

Presentation Skills: Designing an effective Presentation, Contents, appearance, themes in a presentation; Tone and Language in a presentation, Role and Importance of different tools for effective presentation

UNIT V

Motivation/ Inspiration: Ability to shape and direct working methods according to self-defined criteria;Ability to think for oneself, Apply oneself to a task independently with self-motivation, Motivation techniques: Motivation techniques based on needs and field situations

UNIT VI

Self-management, Self-evaluation, Self-discipline, Self-criticism, Recognition of one's own limits and deficiencies, dependency etc. Self-awareness, Identifying one's strengths and weaknesses, Planning & Goal setting, Managing self-emotions, ego, pride leadership & Team dynamics

TEXTBOOKS /REFERENCE:

1. Mitra, Barun, Personality Development and Soft Skills, Oxford University Press, 2016.
2. Ramesh, Gopalswamy, The Ace of Soft Skills: Attitude, Communication and Etiquette for Success, Pearson Education, 2013.
3. Covey, Stephen R., Seven Habits of Highly Effective People: Powerful Lessons in Personal Change, Simon and Schuster, 09-Nov-2004
4. Rosenberg Marshall B., Nonviolent Communication: A Language of Life, PuddleDancer Press, 01-Sep-2003

PG LAB-I

Weekly Teaching Hours	TH: --		Practical: 03	
Scheme of Marking	TH: --	IA: 25	PR/OR: 25	Total: 50

Practical's of the Lab - I shall be based on the courses of first semester. The lab work shall consists of hands on experiments on the different software and hardware platforms related to the syllabus.

PRODUCT DESIGN & QUALITY MANAGEMENT

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide a foundation in product development process
B	To provide a foundation in Quality principles and tools
C	To practice in the application of product development process and quality concepts in real life scenario

Course Outcomes:

CO1	Learner will be able to understand the product development process
CO2	Learner will be able to apply the quality principles and tools for continuous process improvement and problem solving
CO3	Learner will acquire knowledge of tools and techniques for quality managment

UNIT I

Product Design and Development: I Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design.

UNIT II

Product Design and Development: II Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property

UNIT III

Product Development Economics, Managing Product Development Projects.

UNIT IV

Total Quality Management I Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement.

UNIT V

Tools and Techniques: Statistical Process Control, Quality Systems, Bench Marking.

UNIT VI

Total Quality Management II Quality Function Deployment, Product Liability, Failure Mode and Effect Analysis, Management Tools.

Textbooks / References:

1. Dale H. Besterfield,Total Quality Management, Second edition Pearson Education Asia

2. Karl T Ulrich & Steven D Eppinger, Product Design & Development; Third edition, Mc Graw Hill

EMBEDDED OS & RTOS

Weekly Teaching Hours	TH : 03	Tut: 01		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide understanding of the techniques essential to the design and implementation of device drivers and kernel internals of embedded operating systems.
B	To provide the students with an understanding of the aspects of the Real-time systems and Real-time Operating Systems.
C	To provide an understanding of the techniques essential to the design and implementation of real-time embedded systems.

Course Outcomes:

CO1	Learner will understand the Embedded Real Time software that is needed to run embedded systems
CO2	Learner will understand the open source RTOS and their usage.
CO3	Learner will understand the VxWorks RTOS and realtime application programming with it
CO4	Learner will be able to build device driver and kernel internal for Embedded OS & RTOS

UNIT I

Embedded OS (Linux) Internals Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication – Semaphore, Pipes, FIFO,

UNIT II

Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling. Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

UNIT III

Open source RTOS Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS. POSIX standards, RTOS Issues – Selecting a Real Time Operating System, RTOS comparative study.

UNIT IV

Converting a normal Linux kernel to real time kernel, Xenomai basics. Overview of Open source RTOS for Embedded systems (Free RTOS/ ChibiosRT) and application development.

UNIT V

VxWorks / Free RTOS VxWorks/ Free RTOS Scheduling and Task Management – Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems – General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral

UNIT VI

Case study Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

Textbooks / References:

1. Venkateswaran Sreekrishnan, Essential Linux Device Drivers,

2. J. Cooperstein, Writing Linux Device Drivers: A Guide with Exercises,

3. Qing Li, Elsevier, Real Time Concepts for Embedded Systems –

1. Raj Kamal, Embedded Systems Architecture Programming and Design: Tata McGraw Hill

2. Prasad, Embedded/Real Time Systems Concepts, Design and Programming Black Book, KVK

3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society

4. Jane Liu Real-time Systems, PH 2000

5. Laplante, Phillip A, Real-Time Systems Design and Analysis : An Engineer's Handbook:

6. Ward, Paul T & Mellor, Stephen J Structured Development for Real - Time Systems V1 : Introduction and Tools:

7. Ward, Paul T & Mellor, Stephen J Structured Development for Real - Time Systems V2 : Essential Modeling Techniques:

8. Ward, Paul T & Mellor, Stephen J Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques:

9. Simon, David E.Embedded Software Primer:

ELECTIVE-III

FPGA SYSTEM DESIGN

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	The goal is to enable students to design and implement custom computing systems with FPGAs. Students will gain knowledge and understanding of different technologies to implement digital computing systems. Various FPGA architectures. Automated design flows supporting designs with FPGAs. Fundamentals of the FPGA design tools. The reconfigurable computing systems and the roles of FPGAs in those systems.

Course outcomes

CO1	Learner will be able to Translate a software application into hardware logic for FPGA architectures
CO2	Learner will be able to Design synthesizable VHDL systems based on industry-standard coding methods.
CO3	Learner will be able to Optimize logic for various performance goals (timing, frequency, area, and power).
CO4	Learner will be able to Simulate and compare performance results between different optimizations.
CO5	Learner will be able to Utilize commercial FPGA development tools for compilation, simulation, and synthesis.

UNIT I

Introduction to Asics, CMOS Logic and ASIC Library Design

Types of ASICs - Design Flow - CMOS transistors, CMOS design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - transistors as resistors - transistor parasitic capacitance - Logical effort - Library cell design - Library architecture

UNIT II

Programmable Logic Cells and I/O Cells

Digital clock Managers-Clock management- Regional clocks- Block RAM – Distributed RAM Configurable Logic Blocks-LUT based structures – Phase locked loops- Select I/O resources –Anti fuse - static RAM - EPROM and EEPROM technology.

UNIT III

Device Architectures

Device Architecture-Spartan 6 -Vertex 4 architecture- Altera Cyclone and Quartus architectures

UNIT IV

Design Entry and Testing

Logic synthesis using HDL- Types of simulation –Faults- Fault simulation - Boundary scan test - Automatic test pattern generation. Built-in self test. – scan test.Lab exercises.

UNIT V

Floor Planning, Placement And Routing System partition - FPGA partitioning - partitioning methods - floor planning - placement

UNIT VI

Physical design flow - global routing - detailed routing - special routing - circuit extraction – DRC

Textbooks / References:

1. M.J.S. SMITH, “Application Specific Integrated Circuits”, Pearson Education, 2006.

2. Ronald Sass and Andrew G. Schmidt, “Embedded systems design with platform FPGAs: Principles and practices”, Morgan Kaufmann, 2010.

3. Design manuals of Altera, Xilinx and Actel.

Elective-III

WIRELESS SENSOR NETWORK DESIGN

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of design and implementation of WSN
B	To provide ability to formulate and solve problems creatively in the area of WSN
C	To provide in-depth understanding of various applications of WSN.

Course Outcomes:

CO1	Learner will be able to understand the need of WSN and also will analyze the challenges in creating WSN
CO2	Learner will be able to design the architecture of WSN
CO3	Learner will be able to analyze the power and security constraints in WSN
CO4	Learner will be able to understand different operating system to operate WSN
CO5	Learner will be able to understand the basic functioning of WSN at physical layer
CO6	Learner will be able to understand different protocols at network layer to for multiple channel accessing

UNIT I

Introduction: Motivation for a Network of Wireless Sensor Nodes , Sensing and Sensors, Wireless Networks, Challenges and Constraints. Applications: Health care, Agriculture, Traffic and others.

UNIT II

Architectures: Node Architecture, the sensing subsystem, processor subsystem, communication, interface, LMote, XYZ, Hogthrob node architectures

UNIT III

Power Management-Through local power, processor, communication subsystems and other means, time Synchronization need, challenges and solutions overview for ranging techniques Security Fundamentals, challenges and attacks of Network Security, protocol mechanisms for security.

UNIT IV

Operating Systems-Functional and non functional Aspects, short overview of prototypes – TinyOS, SOS, Contiki, Lite OS, sensor grid.

UNIT V

Physical Layer –Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation

UNIT VI

Medium Access Control–types, protocols, standards and characteristics, challenges, Network Layer-Routing Metrics, different routing techniques.

Textbooks / References:

1. Dargie, W. and Poellabauer, C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons, 2010
2. Sohraby, K., Minoli, D., Znati, T. "Wireless sensor networks: technology, protocols, and applications, John Wiley and Sons", 2007
3. Hart, J. K. and Martinez, K. (2006) Environmental Sensor Networks: A revolution in the earth system science? Earth-Science Reviews, 78.
4. Holger Karl, Andreas Willig, Protocols and Architectures for Wireless Sensor Networks--08-Oct 2007

ELECTIVE-III

VLSI AND MICROSYSTEMS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in depth understanding of the principals involved in the latest hardware required for designing and critically analyzing electronic circuits relevant to industry need and society
B	To provide in depth understanding of micro fabrication process, packaging

Course Outcomes:

CO1	Learner will be able to understand the different abstract levels in Verilog for modeling Digital circuits.
CO2	Learner will be able to understand the designing of combinational and sequential circuits in CMOS
CO3	Learner will be able to understand CMOS analog circuits design
CO4	Learner will be able to understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits
CO5	Learner will be able to understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers
CO6	Learner will be able to understand implementation of finite element method for different semiconductor devices

UNIT I

VHDL Modeling and PLD Architectures

Data objects, Data types, Entity, Architecture & types of modeling, Sequential statements, Concurrent statements, Packages, Sub programs, Attributes, VHDL Test bench, Test benches using text files. VHDL modeling of Combinational, Sequential logics & FSM, Meta-stability, PROM, PLA, PAL: Architectures and applications. Software Design Flow, CPLD Architecture, Features, Specifications, Applications. FPGA Architecture, Features, Specifications, Applications.

UNIT II

SoC, Interconnect and Digital CMOS Circuits

Clock skew, Clock distribution techniques, clock jitter. Supply and ground bounce, power distribution techniques. Power optimization. Interconnect routing techniques; wire parasitic, Signal integrity issues. I/O architecture, pad design, Architectures for low power, MOS Capacitor, MOS Transistor theory, C-V characteristics, Non ideal I-V effects, Technology Scaling. CMOS inverters, DC transfer characteristics, Power components, Power delay product. Transmission gate. CMOS combo logic design. Delays: RC delay model, Effective resistance, Gate and diffusion capacitance, Equivalent RC circuits; Linear delay model, Logical effort, Parasitic delay, Delay in a logic gate, Path logical efforts.

UNIT III

Analog CMOS Design and Testability

Current sink and source, Current mirror. Active load, Current source and Push-pull inverters. Common source, Common drain, Common gate amplifiers, Cascode amplifier, Differential amplifier, Operational amplifier, Types of fault, Need of Design for Testability (DFT), Testability, Fault models, Path sensitizing, Sequential circuit test, BIST, Test pattern generation, JTAG & Boundary scan, TAP Controller.

UNIT IV

Microfabrication processes

Glimpses of Microsystems, scaling effects, Smart materials and systems: an overview, Microsensors: some examples, Microactuators: some examples, Microsystems: some examples, Examples of smart systems: structural health monitoring and vibration control, Structure of silicon and other materials, Silicon wafer processing; Thin-film deposition, Lithography, wet etching and dry etching Bulk micromachining and Surface micromachining, Wafer-bonding; LIGA and other moulding techniques, Soft lithography and polymer processing, Thick-film processing; Low temperature co-fired ceramic Processing, Smart material processing.

UNIT V

Mechanics of Solids

Stresses and deformation: bars and beams, Micro device suspensions: lumped modeling, Residual stress and stress gradients, Poisson effect; Anticlastic curvature; examples of micromechanical structures, Thermal loading; bimorph effect, Dealing with large displacements; in-plane and 3D elasticity equations, Vibrations of bars and beams, Gyroscopic effect, Frequency response; damping; quality factor, Basic micro-flows for damping calculation.

UNIT VI

Finite element method and Electronics and packaging

Types of numerical methods for solving partial differential equations, finite element method, Variational principles, Weak form; shape functions, Isoparametric formulation and numerical integration, Implementation of the finite element method, FEM for piezoelectrics, Semiconductor devices: basics, OpAms and OpAmp circuits, Signal conditioning for microsystems devices, Control and microsystems, Vibration control of a beam, Integration of microsystems and microelectronics, Packaging of Microsystems: why and how, Flip-chip, ballgrid, etc., reliability, Case-study 1 (Pressure sensor), Case-study 2 (Accelerometer)

Textbooks / References:

1. K. Eshraghian Eshraghian. D, A. Pucknell, Essentials of VLSI Circuits and Systems, , 2005, PHI. 2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.
2. Ming-BO Lin, Introduction to VLSI Systems: A Logic, Circuit and System Perspective –CRC Press, 2011.
3. N.H.E Weste, K. Eshraghian, Principals of CMOS VLSI Design –, 2nd Ed., Addison Wesley.

ELECTIVE III

INFORMATION SECURITY

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide students with concepts of computer security, cryptography, digital money, secure protocols, detection and other security techniques.

Course Outcomes:

CO1	Learner will acquire knowledge of various data hiding techniques
CO2	Learner will be able identify malicious/harmful programs and concept of firewall
CO3	Learner will be able to express OSI layer and protocols and IP security
CO4	Learner will be able to interpret authentication applications
CO5	Learner will be able to relate security protocols to wireless networks

UNIT I

Cryptography Introduction to Cryptography: OSI Security Architecture - Security Services, Security Attacks, Security Mechanism. Introduction to Classical Cryptography. Modern Cryptography: Secret key Cryptography - DES, AES. Public key Cryptography - DiffieHellman, RSA, ECC. Introduction to Hash Algorithm, Introduction to Digital Signature, Introduction to PKI.

UNIT II

System Security Introduction - Access Control, Intrusion Detection and Prevention. Firewalls: Firewall Design Principles - Firewall Characteristics, Types of Firewalls. Trusted System. Malicious Soft wares: Virus, Trojan Horse, Ad ware/ Spy ware, Worms, Logic Bomb. Cyber Law and Forensics - IT ACT 2000, Cyber Forensics.

UNIT III

Network Security Introduction to Network Concepts, OSI Layers and Protocols, Network Devices, Network layer Security (IPSec) - IP Security Overview, IPSec Architecture, Authentication header, Encapsulating security Payload, Combining Security Associations, Key management.

UNIT IV

Transport Layer Security - SSL/TLS, SET. Application Layer Security - Authentication Applications, Kerberos, X. 509 Authentication Services. E-mail Security – PGP, S/MIME.

UNIT V

Embedded Security Introduction, Types of Security Features – Physical, Cryptographic, Platform. Kinds of Devices – CDC, CLDC. Embedded Security Design, Keep It Simple and

Stupid Principle, Modularity Is Key, Important Rules in Protocol Design, Miniaturization of security, Wireless Security, Security in WSN.

Textbooks / References:

1. William Stallings Cryptography and Network Security: Principles and Practice-
2. Timothy Stapko, Publisher Newnes.Practical Embedded Security: Building Secure Resource Constrained Systems -
3. SD Stinson, Cryptography: Theory and Practice – 3rd Ed. CRC Press.
4. Information Security for Technical Staff-SEI.
5. Guide to firewalls & network security: with intrusion detection & VPNs- HOLDEN, GREG.
6. CISSP: Certified Information Systems Security Professional Study Guide- Stewart, James Michael Et Al.

ELECTIVE IV

ASIC AND SOC

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
B	To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
C	To give the student an understanding of basics of System on Chip and Platform based design.

Course Outcomes:

CO1	Learner will be able to demonstrate VLSI tool-flow and appreciate FPGA architecture.
CO2	Learner will be able to understand the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
CO3	Learner will be able to understand the algorithms used for ASIC construction
CO4	Learner will be able to understand the basics of System on Chip
CO5	Learner will be able to tackle system level design issues

Unit I

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

Unit II

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC, ASIC Construction – Floor planning & placement – Routing

Unit III

System on Chip Design Process: A canonical SoC design, SoC Design Flow – Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process,

Unit IV

System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues;

Unit V

Verification Strategy On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies. MPSoCs. Techniques for designing MPSoCs

Unit VI

SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.

Textbooks / References:

1., Prakash Rashinkar, Peter Paterson and Leena Singh. Kluwer, SoC Verification-Methodology and Techniques, Academic Publishers, 2001.

2. Michael Keating, Pierre Bricaud, Kluwer, Reuse Methodology manual for System-On-A-Chip Designs Academic Publishers, second edition, 2001

3. Smith, Application Specific Integrated Circuits, Addison-Wesley,2006

ELECTIVE-IV

RECONFIGURABLE COMPUTING

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To learn the basics of field of reconfigurable computing
B	To learn Advance digital design skills by developing a reconfigurable computing application Learn a hardware design language Chisel - An introduction to research methodology

Course Outcomes:

CO1	Learner will be able to understand concept of static and dynamic reconfiguration.
CO2	Learner will be able to use the basics of the PLDs for designing reconfigurable circuits.
CO3	Learner will be able to understand the reconfigurable system design using HDL
CO4	Learner will be able to demonstrate different architectures of reconfigurable computing.
CO5	Learner will be able to understand different applications of reconfigurable computing

UNIT I

Types of computing and introduction to RC: General Purpose Computing, Domain-Specific Processors, Application Specific Processors; Reconfigurable Computing, Fields of Application; Reconfigurable Device Characteristics, Configurable, Programmable, and Fixed-Function Devices; General-Purpose Computing, General-Purpose Computing Issues;

UNIT II

Metrics: Density, Diversity, and Capacity; Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement

UNIT III

Routing; Computing Elements, LUTs, LUT Mapping, ALU and CLBs; Retiming, Fine-grained & Coarse-grained structures; Multi-context;

UNIT IV

Different architectures for fast computing viz. PDSPs, RALU, VLIW, Vector Processors, Memories, CPLDs, FPGAs, Multi-context FPGA, Partial Reconfigurable Devices; Structure

and Composition of Reconfigurable Computing Devices: Interconnect, Instructions, Contexts, Context switching, RP space model;

UNIT V

Reconfigurable devices for Rapid prototyping, Non-frequently reconfigurable systems, Frequently reconfigurable systems; Compile-time reconfiguration, Run-time reconfiguration

UNIT VI

Architectures for Reconfigurable computing: TSFPGA, DPGA, Matrix; Applications of reconfigurable computing: Various hardware implementations of Pattern Matching such as the Sliding Windows Approach, Automaton-Based Text Searching. Video Streaming

Textbooks / References:

1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing".
2. IEEE Journal papers on Reconfigurable Architectures.
3. "High Performance Computing Architectures" (HPCA) Society papers.
4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication.
5. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication

ELECTIVE-IV

ELECTRONIC PACKAGING

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To sensitize the undergraduate students and graduate students to the all-important multidisciplinary area of electronics systems packaging.

Course Outcomes:

CO1	Learner will be able to describe the functions and applications of packages and materials used for packaging
CO2	Learner will be able to explain the procedure used for evaluating the electrical aspects of packaging
CO3	Learner will be able to describe component of CAD packages
CO4	Learner will be able to explain the technique used for fabrication and characteristics of single layer and multi-layer PCBs and compare their performances
CO6	Learner will be able to describe about thermal management techniques for packages and reliability of packages

UNIT I

Overview of electronic systems packaging, Definition of a system and history of semiconductors , Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications , Definition of PWB. Video on "Sand-to-Silicon" ,Wafer fabrication, inspection and testing , Wafer packaging; Packaging evolution; Chip connection choices , Wire bonding, TAB and flipchip-1 ,Wire bonding, TAB and flipchip-2.

UNIT II

Necessary of packaging. Types , Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging , Multichip modules (MCM)-types; Systeminpackage (SIP);Packaging roadmaps; Hybrid circuits; Electrical Issues – I; Resistive Parasitic , Electrical Issues – II; Capacitive and Inductive Parasitic , Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.

UNIT III

Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights , Design Flow considerations; Beginning a circuit design with schematic work and component layout , Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for

Reliability. Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued

UNIT IV

Video highlights; Surface preparation, Photoresist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; Resist stripping; Screenprinting technology, Through-hole manufacture process steps; Panel and pattern plating methods. Video highlights on manufacturing; Solder mask for PWBs; Multilayer PWBs; Introduction to microvias, Microvia technology and Sequential build-up technology process flow for high-density interconnects, Conventional Vs HDI technologies; Flexible circuits; Tutorial session.

UNIT V

SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave solderin, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues.

UNIT VI

Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.

Textbooks / References:

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001.
2. William D.Brown,Advanced Electronic Packaging, IEEE Press, 1999.

ELECTIVE IV

ROBOTICS AND MACHINE VISION

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives

A	To familiarize students with the concepts and techniques of robot manipulator, its kinematics, programming and build confidence to evaluate, choose and incorporate
B	robots in engineering systems.

Course Outcome:

CO1	Learner will be able to express basic concept of robotics
CO2	Learner will be able to locate industrial applications of robots
CO3	Learner will be able to distinguish between human vision and machine vision
CO4	Learner will be able to perform image processing techniques and transformation
CO5	Learner will be able to perform image analysis

UNIT I

Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations

UNIT II

Industrial Applications of Robots, and Programming

UNIT III

Principles of Machine Vision, Vision and factory automation, Human Vision Vs. Machine Vision, Economic Considerations, Machine Vision – System Overview, Image acquisition – Illumination, Image formation and Focusing, Image Detection – Introduction, Types of Cameras; Image Processing and Presentation.

UNIT IV

Image Processing Techniques and Transformations: Fundamental Concepts of Image Processing, Pixel, Pixel Location. Gray Scale, Quantizing Error and Measurement Error and Histograms.

UNIT V

Basic Machine Vision Processing Operators – Monadic one Point Transformations: Identity operator, Inverse Operator, Threshold operator and other operators via: Inverted Threshold operator, Binary Threshold operator, Inverted Binary Threshold Operator, Gray Scale Threshold and Inverted Gray Scale Threshold Operators; Dyadic Two Point Transformations – Image Addition, Image Subtracting, Image Multiplication; Convolution and Spatial Transformations

UNIT VI

Edge Enhancement Techniques and Image Analysis: Introduction, Digital Filters – Low pass and High Pass filters; Edge Enhancement Operators – Laplacian, Roberts Gradient, Sobel and other Local operators. Image Analysis: Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm.

Textbooks / References:

1. Louis J. Galbiati, Jr.Machine Vision and Digital Image Processing, Prentice Hall, Englewood Cliffs, New Jersy.
2. Yoram Koren Robotics for Engineers, McGraw Hill.
3. Janakiraman P. A., Robotics and Image Processing – an Introduction, Tata McGraw Hill, New Delhi
4. Robert J.Schalkoff, Digital Image Processing and Computer Vision, John Wiley & Sons Inc.
5. Mikell P. Groover, Mitchell Wein, Roger N. Nagel and Nicholas G. Odlrey, Industrial Robotics – Technology, Programming and Applications, McGraw Hill International Edistion.
6. Klette, Reinhard & Zamperoni, Piero; Handbook Of Image Processing Operators, John Wiley & Sons Inc
7. Sonka, Milan Et Al, Image Processing, Analysis And Machine Vision
8. Hodges, Bernard,Industrial Robotics by Jaico Publishing House, Delhi
9. Adrian Low,Introductory Computer Visiona dn Image Processing by McGraw Hill International Editions.

ELECTIVE V

INTERNET OF THINGS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	Students will be explored to the interconnection and integration of the physical world and the cyber space.
B	To provide ability to design and develop IOT devices.

Course Outcomes:

CO1	Learner will be able to understand the meaning of internet in general and IOT in terms of layers, protocols, packets peer to peer communication
CO2	Learner will be able to interpret IOT working at transport layer with the help of various protocols
CO3	Learner will be able to understand IOT concept at data link layer
CO4	Learner will be able to apply the concept of mobile networking to the internet connected devices
CO5	Learner will be able to measure and schedule the performance of networked devices in IOT
CO6	Learner will be able to analyze the challenges involve in developing IOT architecture

UNIT I

Introduction: What is the Internet of Things: History of IoT, about objects/things in the IoT, Overview and motivations, Examples of applications, IoT definitions, IoT Frame work, General observations, ITU-T views, working definitions, and basic nodal capabilities.

UNIT II

Fundamental IoT Mechanisms & Key Technologies : Identification of IoT objects and services, Structural aspects of the IoT, Environment characteristics, Traffic characteristics ,scalability, Interoperability, Security and Privacy, Open architecture, Key IoT Technologies ,Device Intelligence, Communication capabilities, Mobility support, Device Power, Sensor Technology, RFID technology, Satellite Technology.

UNIT III

Radio Frequency Identification Technology: Introduction, Principles of RFID, Components of an RFID system, Reader, RFID tags, RFID middleware, Issue. Wireless Sensor Networks: History and context, node, connecting nodes, networking nodes, securing communication.

UNIT IV

Wireless Technologies For IoT : Layer ½ Connectivity : WPAN Technologies for IoT/M2M, Zigbee /IEEE 802.15.4, Radio Frequency for consumer Electronics (RF4CE), Bluetooth and

its low-energy profile , IEEE 802.15.6 WBANS, IEEE 802.15 WPAN TG4j, MBANS, NFC, dedicated short range communication(DSRC) & related protocols. Comparison of WPAN technologies cellular & mobile network technologies for IoT/M2M.

UNIT V

Governance of The Internet of Things: Introduction, Notion of governance, aspects of governance, Aspects of governance Bodies subject to governing principles, private organizations, International regulation and supervisor, substantive principles for IoT governance, Legitimacy and inclusion of stakeholders, transparency, accountability. IoT infrastructure governance, robustness, availability, reliability, interoperability, access. Future governance issues, practical implications, legal implications.

UNIT VI

Internet of Things Application Examples: Smart Metering, advanced metering infrastructure, e-Health/Body area network, City automation, automotive applications. Home automation, smart cards, Tracking, Over-The-Air passive surveillance/Ring of steel, Control application examples.

Textbooks / References:

1. Hakima Chaouchi, The Internet of Things, Connecting Objects to the Web, Wiley Publications
2. Daniel Minoli,Building the Internet of Things with IPv6 and MIPv6 The Evolving World of M2M Communications, Wiley Publications
3. Bernd Scholz-Reiter, Florian Michahelles, Architecting the Internet of Things, ISBN 978- 3842-19156-5, Springer.
4. Olivier Hersent, David Boswarthick, Omar Elloumi, The Internet of Things Key Applications and Protocols, ISBN 978-1-119-99435-0, Wiley Publications.

ELECTIVE V

LINEAR ALGEBRA

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of fundamental concepts of linear algebra
B	To understand the importance of linear algebra and learn its applicability to practical problems

Course Outcomes:

CO1	Student will learn to solve and analyze linear system of equation
CO2	Student will analyze the direct notations, duality, adjointness, bases, dual bases in linear algebra
CO3	Student will understand the concept of Linear transformations and matrices, equivalence, similarity.
CO4	Student will be able to find eigen values and eigen vectors using characteristics polynomials
CO5	Student will learn to find the singular value decomposition of the matrix
CO6	Student will be to find the inverse of matrix

UNIT I

Fields Fq, R, C. Vector Spaces over a field, Fn, F[ɵ]=Polynomials in one Variable.

UNIT II

Direct Notations, Ket, bra vector, duality, adjointness, linear transformations, bases, dual bases.

UNIT III

Linear transformations and matrices, equivalence, similarity.

UNIT IV

Eigenvalues, eigenvectors, diagonalization, Jordoncanonical form

UNIT V

Bilinear and sesquilinear forms, inner product, orthonormal, bases, orthogonal decomposition, projections

UNIT VI

System of equations, generalized inverses.

Textbooks / References:

1. Ronald Shaw, Linear Algebra and Group Representations, AcademicPress, Volume I-1982.

2. Ronald Shaw, Linear Algebra and Group Representations, AcademicPress,Volume II-1983.

3. A. R. Rao, BhimaSankaran, Linear Algebra, TRIM, 2nd Edition, Hindustan

ELECTIVE V

NEURAL NETWORKS IN EMBEDDED APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To be able to use analogy of human neural network for understanding of artificial learning algorithms.
B	To give in-depth understanding of fundamental concepts of neural network
C	To exhibit the knowledge of radial basis function network

Course Outcomes:

CO1	Learner will be able to understand concept of fuzzy logic.
CO2	Learner will be able to understand embedded digital signal processor, Embedded system design and development cycle, applications in digital camera
CO3	Learner will be able to understand embedded systems, characteristics, features and applications of an embedded system
CO4	Learner will be able to design and utilization of fuzzy logic controller for various industrial applications
CO5	Learner will be able to implement of radial basis function, neural network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

UNIT I

Introduction to artificial neural networks, Fundamental models of artificial neural network, Perceptron networks, feed forward networks, Feedback networks, Radial basis function networks, Associative memory networks

UNIT II

Self-organizing feature map, Learning Vector Quantization, Adaptive resonance theory, Probabilistic neural networks, neocgnitron, Boltzmann Machine.

UNIT III

Optical neural networks, Simulated annealing, Support vector machines, Applications of neural network in Image processing,

UNIT IV

Introduction to Embedded systems, Characteristics, Features and Applications of an embedded system

UNIT V

Introduction to embedded digital signal processor, Embedded system design and development cycle, ANN application in digital camera,

UNIT VI

Implementation of Radial Basis Function, Neural Network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

Textbooks / References:

1. S N Sivanandam, S Sumathi, S N Deepa, "Introduction to Neural Networks Using Matlab 6.0", Tata McGraw Hill Publication
2. Simon Haykin, "Neural Networks: Comprehensive foundation", Prentice Hall Publication
3. Frank Vahid, TonyGivargis, "Embedded System Design A unified Hardware/ Software Introduction", Wiley India Pvt. Ltd.
4. Rajkamal, "Embedded Systems Architecture, Programming and Design," Tata McGraw-Hill

ELECTIVE V

RESEARCH METHODOLOGY

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To develop a research orientation among the scholars and to acquaint them with fundamentals of research methods.
B	To develop understanding of the basic framework of research process.
C	To identify various sources of information for literature review and data collection.
D	To understand the components of scholarly writing and evaluate its quality.

Course Outcomes:

CO1	Student will learn the meaning, objective , motivation and type of research
CO2	Student will be able to formulate their research work with the help of literature review
CO3	Student will be able to develop an understanding of various research design and techniques
CO4	Student will have an overview knowledge of modeling and simulation of research work
CO5	Student will be able to collect the statistical data with different methods related to research work
CO6	Student will be able to write their own research work with ethics and non-plagiarized way

UNIT I

Introduction: Defining research, Motivation and Course Objective:s, Types of research

Meaning of Research, Course Objective:s of Research, Motivation in Research, Types of Research

UNIT II

Research Formulation: Formulating The research Problem, Literature Review, Development of Working Hypothesis

UNIT III

Research Design: Important Concept in Research Design, Research Life Cycle, Developing Research Plan

UNIT IV

Overview of Modeling and Simulation: Classification of models, Development of Models, Experimentation, Simulation.

UNIT V

Statistical Aspects: Methods of Data Collection, Sampling Methods, Statistical analysis, Hypothesis testing.

UNIT VI

Research Report: Research Ethics, Plagiarism, Research Proposal, Report Writing and Writing Research Papers.

Textbooks / References:

1. J.P. Holman. ,Experimental Methods for Engineers
2. C.R. Kothari, Research Methodology, Methods & Techniques

ELECTIVE V

WAVELET TRANSFORMS AND ITS APPLICATIONS

Weekly Teaching Hours	TH : 03	Tut: --		
Scheme of Marking	TH :60	Tests : 20	IA: 20	Total : 100

Course Objectives:

A	To provide in-depth understanding of fundamental concepts of Wavelets.
B	To study wavelet related constructions, its applications in signal processing, communication and sensing.

Course Outcomes:

CO1	Learner will be able to understand the meaning of wavelet transform
CO2	Learner will be able to understand the terminologies used in Wavelet transform with its properties
CO3	Learner will be able to demonstrate various filter bank using wavelet transformation
CO4	Learner will be able to understand bases , orthogonal bases in wavelet transform
CO5	Learner will be able to understand different types of wavelet transform
CO6	Learner will be able to design practical system using wavelet transform

UNIT I

Continuous Wavelet Transform Introduction, Continuous-time wavelets, Definition of the CWT, the VWT as a Correlation, Constant-Factor Filtering Interpretation and Time-Frequency Resolution, the VWT as an Operator, Inverse CWT, Problems.

UNIT II

Introduction to Discrete Wavelet Transform And Orthogonal Wavelet Decomposition: Introduction, Approximation of Vectors in Nested Linear Vector Subspaces, Examples of an MRA, Problems.

UNIT III

MRA, Orthonormal Wavelets, And Their Relationship To Filter Banks: Introduction, Formal Definition of an MRA, Construction of General Orthonormal MRA, a wavelet Basic for the MRA,

UNIT IV

Digital Filtering Interpretation, Examples of Orthogonal Basic Generating Wavelets, Interpreting Orthonormal MRAs for Discrete-Time signals, Miscellaneous Issues Related to

PRQME Filter Banks, generating Scaling Functions and wavelets from Filter Coefficient, Problems.

UNIT V

Wavelet Transform And Data Compression: Introduction, Transform Coding, DTWT for Image Compression, Audio Compression, And Video Coding Using Multiresolution Techniques: a Brief Introduction.

UNIT VI

Other Application 0f Wavelet Transforms: Introduction, Wavelet denoising speckles Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transform of Projections, Communication application.

Textbooks / References:S

1. C. Sidney Burrus, R. A. Gopianath, Pretice Hall, Introduction to Wavelet and Wavelet Transform
2. P.P.Vaidyanathan , PTR Prentice Hall, Englewood Cliffs , New Jersey, Multirate System and Filter Banks
3. N.J.Fliege , John Wiley & Sons, Multirate Digital Signal Processing
4. Raghuveer Rao, Ajit Bopardikar, Pearson Education Asia,Wavelet Transforms Introduction to Theory and Application
5. James S. Walker, "A Primer on Wavelets and their Scientific Applications", CRC Press, (1999).
6. Rao, "Wavelet Transforms", Pearson Education, Asia.

SEMINAR I

Weekly Teaching Hours	TH: -	Practical: 04	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The seminar shall be on the state of the art in the area of the wireless communication and computing and of student's choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.

MINI PROJECT

Weekly Teaching Hours	TH: -	Practical: 04	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The mini project shall be based on the recent trends in the industry, research and open problems from the industry and society. This may include mathematical analysis, modelling, simulation, and hardware implementation of the problem identified. The mini project shall be of the student's choice and approved by the guide. The student has to submit the report of the work carried out in the prescribed format signed by the guide and head of the department/institute.

PROJECT MANAGEMENT AND INTELLECTUAL PROPERTY RIGHTS

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

The Student has to choose this course either from NPTEL/MOOCs/SWAYAM pool. It is mandatory to get the certification of the prescribed course.

PROJECT-I

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 50	PR/OR: 50	Total: 100

Project-I is an integral part of the final project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation that may include mathematical model/SRS/UML/ERD/block diagram/ PERT chart, and layout and design of the proposed system/work. As a part of the progress report of project-I work, the candidate shall deliver a presentation on progress of the work on the selected dissertation topic.

It is desired to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall submit the duly certified progress report of project -I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.

PROJECT-II

Weekly Teaching Hours	TH: -	Practical: -	
Scheme of Marking	IA: 100	PR/OR: 100	Total: 200

In Project - II, the student shall complete the remaining part of the project which will consist of the simulation/ analysis/ synthesis/ implementation / fabrication of the proposed project work, work station, conducting experiments and taking results, analysis and validation of results and drawing conclusions.

It is mandatory to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.