Course Structure and Syllabus

For

M. Tech. (Embedded Engineering)

Two Year (Four Semester) Course

(w.e.f. July 2017)
M. Tech. (Embedded Engineering)

Objectives

I. To serve the society and nation, by providing high quality engineering educational programs to the students, engaging in research and innovations that will enhance the skill and knowledge and assisting the economic development of the region, state, and nation through technology transfer.

II. To equip the postgraduate students with the state of the art education through research and collaborative work experience/culture to enable successful, innovative, and life-long careers in Electronics and Telecommunication.

III. To encourage the post-graduates students, to acquire the academic excellence and skills necessary to work as Electronics and Telecommunication professional in a modern, ever-evolving world.

IV. To provide the broad understanding of social, ethical and professional issues of contemporary engineering practice and related technologies, as well as professional, ethical, and societal responsibilities.

V. To inculcate the skills for perusing inventive concept to provide solutions to industrial, social or nation problem.

Outcomes

I. Students of this program will have ability to apply knowledge of mathematics, sciences and engineering to Electronics and Telecommunication problems.

II. Postgraduate students will gain an ability to design and conduct experiments, as well as to analyze and interpret data/results.

III. Learners of this program will built an ability to design and develop a system, components, devices, or process to meet desired needs.

IV. Masters students of this program will have an ability to work on multi-disciplinary teams and also as an individual for solving issues related to Electronics and Telecommunication.

V. Learners of this program will have an ability to identify, formulate, and solve Engineering problems by applying mathematical foundations, algorithmic principles, and Electronics and Telecommunication theory in the modeling and design of electronics systems in a way that demonstrates comprehension of the tradeoffs involved in design choices.

VI. Postgraduate students will have an ability to communicate effectively orally and in writing and also understanding of professional and ethical responsibility.

VII. Postgraduate students will have an ability to use the techniques, skills, and modern engineering EDA tools necessary for Electronics and Telecommunication practices.

VIII. Learners of this program will have an ability to evaluate Electronics and Telecommunication Engineering problems with cost effectiveness, features, and user friendliness to cater needs for innovative product development.

IX. Postgraduate students will have an ability to solve contemporary social and industrial problems by engaging in life-long learning.
Dr. Babasaheb Ambedkar Technological University
Teaching and Examination Scheme for
M.Tech. (Embedded Engineering) w.e.f. July 2017

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Course Code</th>
<th>Name of the course</th>
<th>Hours/Week</th>
<th>Credit</th>
<th>Examination scheme</th>
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<td>Advanced Digital System Design</td>
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<td>MTESC201</td>
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<td>Embedded OS and RTOS</td>
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* PG Lab-I—Practical shall be based on courses of first semester.

# Student has to choose this course either from NPTEL/MOOC pool and submission of course completion certificate is mandatory.
Elective-I
A. Artificial Neural Networks and Applications
B. Digital VLSI design
C. Advanced Processors and its applications
D. Fault Tolerant Systems
E. Electromagnetic Interference and Compatibility

Elective-II
A. Design and Analysis of Algorithms
B. System On-Chip
C. Optical Fiber Communication
D. Statistical Signal Processing
E. Microelectronics

Elective-III
A. FPGA System Design
B. Wireless Sensor Network Design
C. VLSI and Microsystems
D. Information Security

Elective-IV
A. ASIC & SOC
B. Reconfigurable Computing
C. Electronic Packaging
D. Robotics and Machine Vision

Elective-V (Open)
A. Internet of Things
B. Linear Algebra
C. Neural Networks in Embedded Applications
D. Research Methodology
E. Wavelet Transforms and its Applications
SYSTEM DESIGN USING EMBEDDED PROCESSORS

Weekly Teaching Hours

<table>
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<tr>
<th>Component</th>
<th>Hours</th>
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Scheme of Marking

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<tr>
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Course Objectives:

| A | To impart the concepts and architecture of Embedded systems and to make the students capable of designing Embedded systems |

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will understand the Concepts and Architecture of Embedded Systems</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Learner will get knowledge of ARM processor</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to describe Cortex-M3 processor</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to compile program with Cortex M3 processor</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to distinguish between different peripherals and debugging tools</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II

UNIT III
Overview of Cortex-M3 Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.

UNIT IV
UNIT V

UNIT VI
Cortex-M3/M4 Microcontroller STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control. STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART. Development & Debugging Tools: Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.

Textbooks / References:
EMBEDDED PROGRAMMING

Weekly Teaching Hours

| TH : 03 | Tut: 01 |

Scheme of Marking

| TH :60 | Tests : 20 | IA: 20 | Total : 100 |

Course Objectives:

| A | This subject is framed to set the required background in embedded system concepts, Fundamentals of Linux OS and “C” language for the rest of the modules. |
| B | It aims at familiarizing the students in embedded concepts and programming in ‘C’. |
| C | This module covers the advanced topics in ‘C’ such as Memory management, |
| D | Pointers, Data structures which are of high relevance in embedded software is considered in depth. |
| E | The syllabus also covers the topic ‘scripting languages for embedded systems’ |

Course Outcomes:

| CO1 | Learner will be able to develop advanced programs in Embedded C |
| CO2 | Learner will be able to get knowledge in Embedded OS (Linux) fundamentals |
| CO3 | Learner will be able to develop programs using scripting languages |
| CO4 | Learner will be able to model and analyze real time embedded systems |
| CO5 | Learner will be able to correlate relevance of programming languages in embedded systems |
| CO6 | Learner will be able to compare scripting languages |

UNIT I
Embedded OS Fundamentals (Linux) Introduction: Operating System Fundamentals, General Linux Architecture, Linux Kernel, Linux file systems, ROOTFS, Sysfs and Procfs,

UNIT II
Embedded Linux: Booting Process in Linux, boot loaders, U-boot, Kernel Images, Linux File systems. GNU Tools: gcc, gdb, gprof, Makefiles

UNIT III
Embedded C Programming Review of data types –scalar types-Primitive types-Enumerated types Subranges, Structure types-character strings –arrays- Functions Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly.

UNIT IV
Embedded programming issues - Reentrancy, Portability, Optimizing and testing embedded C programs. Modelling Language for Embedded Systems: Modeling and Analysis of RealTime and Embedded systems
UNIT V
Embedded Applications using Data structures Linear data structures—Stacks and Queues
Implementation of stacks and Queues-Linked List-Implementation of linked list, Sorting,
Searching, Insertion and Deletion, Nonlinear structures—Trees and Graphs Object Oriented
programming basics using C++ and its relevance in Embedded systems.

UNIT VI
Scripting Languages for Embedded Systems Shell scripting, Programming basics of Python,
Comparison of scripting languages

Textbooks / References:
1. C Programming language, Kernighan, Brian W, Ritchie, Dennis M, Embedded C, Michael
   J. Pont, Addison Wesley
   C for Microcontrollers-A Hands on Approach”, Springer.
3. Daniel W. Lewis, Fundamentals of embedded software where C and assembly meet,
4. Bruce Powel Douglas, Real time UML, second edition: Developing efficient objects for
8. Bjarne Stoustrup, C++ programming language, Addison-Wesley
9. Tom Swan, GNU C++ For LinuxPrentice, Hall India
10. Robert Lafore, Object Oriented programming in C++, Galgotia publications
    Publishers
12. Jones, M Tims GNU/LINUX Application Programming,
ADVANCED DIGITAL SYSTEM DESIGN

Weekly Teaching Hours

TH: 03  Tut: 01

Scheme of Marking

TH: 60  Tests: 20  IA: 20  Total: 100

Course Objectives:

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<tr>
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<tbody>
<tr>
<td>A</td>
<td>To prepare students for the design of practical digital hardware systems using VHDL.</td>
</tr>
<tr>
<td>B</td>
<td>To introduce students to the fundamentals of combination logic design and then to sequential circuits (both synchronous and asynchronous).</td>
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<tr>
<td>C</td>
<td>To provide opportunities to synthesize the designs (using both schematic capture and VHDL) for implementation in FPGAs.</td>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to differentiate combinational and sequential circuits</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to design asynchronous sequential circuits</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to express different aspects VHDL</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to detect faults in logic circuits</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to realize combinational circuits using HDL</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will get knowledge of FPGA</td>
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</table>

UNIT I
Introduction to Digital Design
Combinational Circuit Design, Synchronous Sequential Circuit Design - Mealy and Moore model, State machine design, Analysis of Synchronous sequential circuit, State equivalence, State Assignment and Reduction, Analysis of Asynchronous Sequential Circuit, flow table reduction, races, state assignment

UNIT II
Design of Asynchronous Sequential Circuit, Designing with PLDs – Overview of PLDs – ROMs, EPROMs – PLA – PAL - Gate Arrays – CPLDs and FPGAs, Designing with ROMs - Programmable Logic Arrays - Programmable Array logic, PAL series 16 & 22 – PAL22V10 - Design examples.

UNIT III

UNIT IV
UNIT V

UNIT VI
FPGA - FPGAs - Logic blocks, Routing architecture, Design flow technology - mapping for FPGAs, Xilinx FPGA Architecture, Xilinx XC4000 - ALTERA’s FLEX 8000, Design flow for FPGA Design, Case studies: Virtex II Pro.

Textbooks / References:
2. Geoff Bestock, "FPGAs and programmable LSI; A Designers Handbook", Butterworth Heinemann, 1996
8. Kevin Skahill, "VHDL for Programmable Logic", Addison -Wesley, 1996
ELECTIVE-I
ARTIFICIAL NEURAL NETWORKS AND APPLICATIONS

Weekly Teaching Hours  TH : 03  Tut:  --

Scheme of Marking  TH :60  Tests : 20  IA: 20  Total : 100

Course objectives:

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<td>A</td>
<td>To provide in-depth understanding of fundamental theory and concepts of computational intelligence methods</td>
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<tr>
<td>B</td>
<td>To understand the fundamental theory and concepts of neural networks, neuro-modeling, several neural network paradigms and its applications.</td>
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Course Outcomes:

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<td>CO1</td>
<td>Learner will be able to articulate analogy of human neural network for understanding of artificial learning algorithms.</td>
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<tr>
<td>CO2</td>
<td>Learner will be able to analyze radial basis function network.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze neural network architecture &amp; basic learning algorithms.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand mathematical modeling of neurons, neural networks.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to analyze training, verification and validation of neural network models</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to design Engineering applications that can learn using neural networks</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II
Functions, Mathematical Preliminaries, Artificial Neurons, Neural Networks and Architectures Pattern analysis tasks: Classification, Clustering, mathematical models of neurons, Structures of neural networks, learning principles.

UNIT III
UNIT IV
Auto-associative neural networks, Pattern storage and retrieval, Hopfield model, recurrent neural networks, Bayesian neural networks,

UNIT V
Radial basis function networks: Regularization theory, RBF networks for function approximation, RBF networks for pattern classification

UNIT VI
Self-organizing maps: Pattern clustering, Topological mapping, Kohonen’s self-organizing map Introduction to cellular neural network, Fuzzy neural networks, and Pulsed neuron models recent trends in Neural Networks

Textbooks / References:
**ELECTIVE-I**

**DIGITAL VLSI DESIGN**

Weekly Teaching Hours
TH : 03  Tut:  --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

**Course Objectives:**

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<tbody>
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<td>A</td>
<td>To create models of moderately sized CMOS circuits that realize specified digital functions</td>
</tr>
<tr>
<td>B</td>
<td>Have an understanding of the characteristics of CMOS circuit construction</td>
</tr>
<tr>
<td>C</td>
<td>To complete a significant VLSI design project having a set of objective criteria and design constraints.</td>
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**Course Outcomes:**

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be aware about the trends in semiconductor technology, and how it impacts scaling and performance.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to model moore and melay machine</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to classify complex programmable logic devices</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to extend his knowledge to CMOS subsystem design</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to paraphrase floor planning concept</td>
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**UNIT I**

**Introduction to VLSI Circuits**


**UNIT II**

**Digital Circuit Design using VHDL**

Design of sequential circuits, asynchronous and synchronous design issues, state machine modeling (Moore and mealy machines), packages, sub programs, attributes, test benches.
UNIT III

Programmable Logic Devices

Complex Programmable Logic Devices – Architecture of CPLD, Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT IV

CMOS Subsystem Design

Semiconductor memories, memory chip organization, Random Access Memories (RAM), Static RAM (SRAM), standard architecture, 6T cell, sense amplifier, address decoders, timings. Dynamic RAM (DRAM), different DRAM cells, refresh circuits, timings.

UNIT V

Floor Planning and Placement

Floor planning concepts, shape functions and floor plan sizing, Types of local routing problems, Area routing, channel routing, global routing, algorithms for global routing.

UNIT VI

Fault Tolerance and Testability

Types of fault, stuck open, short, stuck at 1, 0 faults, Fault coverage, Need of Design for Testability (DFT), Controllability, predictability, testability, built in Self Test (BIST), Partial and full scan check, Need of boundary scan check, JTAG, Test Access Port (TAP) controller

Textbooks / References:

5. Data Sheets of PLDs.
6. Sung-Mo (Steve) Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata
ELECTIVE- I
ADVANCED PROCESSORS AND ITS APPLICATIONS

Weekly Teaching Hours
TH : 03    Tut:  --

Scheme of Marking
TH :60    Tests : 20    IA: 20    Total : 100

Course objectives:

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<tbody>
<tr>
<td>A</td>
<td>Architect a microprocessor or microcontroller system and estimate the required hardware and software resources.</td>
</tr>
<tr>
<td>B</td>
<td>Select a microprocessor or microcontroller suitable to the application.</td>
</tr>
<tr>
<td>C</td>
<td>Perform the detailed hardware design of a microprocessor or microcontroller system.</td>
</tr>
<tr>
<td>D</td>
<td>Program the microprocessor or microcontroller using suitable techniques including use of allocation schemes and device drivers.</td>
</tr>
<tr>
<td>E</td>
<td>Find effective solutions to a wide range of real-world microprocessor and microcontroller applications.</td>
</tr>
</tbody>
</table>

Course Outcomes:

| CO1 | Learner will be able to express architecture of typical 8 bit microprocessor |
| CO2 | Learner will be able to summarize various aspects of 16 bit microprocessor |
| CO3 | Learner will be able to interface IO devices to microprocessor              |
| CO4 | Learner will be able to interface analog IO devices to microprocessor      |
| CO5 | Learner will be able to express 8 bit microcontroller and architecture     |

UNIT I
Review of basic microprocessor and microcomputer concepts and the architecture and instruction set of a typical 8 bit microprocessor.

UNIT II
ADVANCED PROCESSORS: - Overview of 16-bit/32-bit/64 bit Intel based microprocessors. Arithmetic and I/O co-processor architecture. Register details, operation-addressing modes & instruction set of a typical 16-bit microprocessor, assembly language programming for the processor introduction to multiprocessing.

UNIT III
PROGRAMMIA BLE SUPPORT CHIPS:- Programmable parallel interface chip (e.g. 8255) functional schematic. Pin function operating mode interface with microprocessor chip programming serial communication interface chip (e.g. 8251) functional schematic pin function.
UNIT IV
Operating mode interface with processor mode and command words for the chip programmable interrupt controller (8259) functional schematic pin function single and cascaded operation interface with microprocessor and I/O devices Programmable interval timer (8253) functional schematic pin functions. Modes of operations.

UNIT V
ANALOG INPUT AND OUTPUT: - Microprocessor compatible ADC &amp; DAC chips interfacing ADC with multiplexer with ADC, microprocessor use of sample and hold circuit interfacing DAC with microprocessor.

UNIT VI
MICROCONTROLLER:- Hardware and software integration in microprocessor control system. An overview of 8-bit microcontroller architecture and instruction set.

Textbooks / References:
1. Advanced Microprocessor A.K.Ray, K.M.Bhurchandi TMH
2. Microprocessor Gaonkar
3. Microprocessor, Hardware &amp; Programming Douglas V Hall
ELECTIVE-I
FAULT TOLERANT SYSTEMS

Weekly Teaching Hours  TH : 03  Tut:  --

Scheme of Marking  TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To provide in-depth understanding of the fundamental concepts of fault-tolerance.</td>
</tr>
<tr>
<td>B</td>
<td>To develop skills in modeling and evaluating fault-tolerant architectures in terms of reliability, availability and safety</td>
</tr>
<tr>
<td>C</td>
<td>To gain knowledge in sources of faults and means for their prevention and forecasting</td>
</tr>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to analyze the risk of computer failures and their peculiarities compared with other equipment failures.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to analyze advantages and limits of fault avoidance and fault tolerance techniques.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to distinguish threat from software defects and human operator error as well as from hardware failures.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to analyze different forms of redundancy and their applicability to different classes of dependability requirements.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to choose among commercial platforms (fault-tolerant or non fault-tolerant) on the basis of dependability requirements.</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to demonstrate the use of fault tolerance in the design of application software.</td>
</tr>
<tr>
<td>CO7</td>
<td>Learner will be able to analyze relevant factors in evaluating alternative system designs for a specific set of requirements.</td>
</tr>
<tr>
<td>CO8</td>
<td>Learner will be aware of the subtle failure modes of &quot;fault-tolerant&quot; distributed systems, and the existing techniques for guarding against them.</td>
</tr>
<tr>
<td>CO9</td>
<td>Learner will be able to analyze cost-dependability trade-offs and the limits of computer system dependability.</td>
</tr>
</tbody>
</table>

UNIT I

Modelling and Logic Simulation:

Functional modelling at the logic and the register level, Structural models, Level of modelling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation, different delay models, Hazard Detection.
UNIT II
Fault Modelling and Fault Simulation:

UNIT III
Compression techniques and self-checking System:
General aspects of compression techniques, ones-count compression, transition –count compression, Parity –check compression, Syndrome testing and Signature Analysis,

UNIT IV

UNIT V
Testability: Testability, trade-offs, Ad hoc Design for Testability techniques, Introduction to BIST concept, Test pattern generation for BIST

UNIT VI
Self-testing circuits for systems, memory & processor testing, PLA-testing, automatic test pattern generation and Boundary Scan Testing JTAG.

Textbooks / References:
ELECTIVE-I
ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

Weekly Teaching Hours | TH: 03 | Tut: --
Scheme of Marking | TH: 60 | Tests: 20 | IA: 20 | Total: 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To familiarize with the fundamentals that are essential for electronics industry in the field of EMI / EMC</td>
</tr>
<tr>
<td>B</td>
<td>To understand EMI sources and its measurements.</td>
</tr>
<tr>
<td>C</td>
<td>To understand the various techniques for electromagnetic compatibility.</td>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will acquire knowledge of EMI / EMC sources and their standards</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to measure different parameters of interference in EM</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to reduce the interference within EM devices</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to illustrate the physical and statistical model of EM devices</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to analyze the EM devices in terms of Computer Based Modeling and Simulation</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to design electronic systems that function without errors or problems related to electromagnetic compatibility.</td>
</tr>
</tbody>
</table>

UNIT I

Introduction to EMI / EMC:

EMI / EMC Standards, Introduction to E, H, Near and far field radiators, Receptors and antennas, Different types of EMI sources and possible remedies.

UNIT II

Measurement techniques in EMI: Open area test sites, Radiated interference measurements, Conducted interference measurements, Interference immunity.

UNIT III

EMI reduction techniques: Grounding, Shielding, Bonding, EMI filters.

UNIT IV

UNIT V

Computer Based Modeling and Simulation: Computer Based Modeling and Simulation of EMI Models and Signal Integrity.

UNIT VI

Electrostatic Discharge (ESD): Introduction, Accumulation of Static Charge on Bodies Charging and Charge Separation, Human Body as Source of ESD, ESD Waveforms, Human Body Circuit Model, ESD Generator and ESD Test

Textbooks / References:
2. Electromagnetic Compatibility, Principles and Applications; Devid A. Weston, Marcel Dekker, Inc New York.
ELECTIVE-II
DESIGN AND ANALYSIS OF ALGORITHMS

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH : 60  Tests : 20  IA: 20  Total : 100

Course Objectives:

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<tr>
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<tbody>
<tr>
<td>A</td>
<td>The student should be made to: Learn the algorithm analysis techniques.</td>
</tr>
<tr>
<td>B</td>
<td>Become familiar with the different techniques.</td>
</tr>
<tr>
<td>C</td>
<td>Understand the limitations of Algorithm power.</td>
</tr>
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Course Outcomes:

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<tr>
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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to Design algorithms for various computing problems.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to Analyze the time and space complexity of algorithms.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to Critically analyze the different algorithm design techniques for a given problem.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to Modify existing algorithms to improve efficiency.</td>
</tr>
</tbody>
</table>

UNIT I
Introduction

UNIT II
Brute Force And Divide-And-Conquer

UNIT III
Dynamic Programming And Greedy Technique

UNIT IV
Iterative Improvement
UNIT V
Coping With The Limitations Of Algorithm Power
Limitations of Algorithm Power-Lower-Bound Arguments-Decision Trees-P, NP and NP-Complete Problems--Coping with the Limitations - Backtracking – n-Queens problem –

UNIT VI

Textbooks / References:
ELECTIVE-II
SYSTEM ON CHIP

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH : 60  Tests : 20  IA: 20  Total : 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To provide students with a sound knowledge of VLSI systems covering the following:</td>
</tr>
<tr>
<td>B</td>
<td>To provide an in-depth understanding of what SoC is and what are the differences between SoC and Embedded System</td>
</tr>
<tr>
<td>C</td>
<td>To provide an in-depth understanding of basics of System on Chip and Platform based design.</td>
</tr>
<tr>
<td>D</td>
<td>To provide an in-depth understanding of issues and tools related to SoC design and implementation.</td>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to interpret nature of hardware and software, its data flow modeling and implementation techniques.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to analyze the micro-programmed architecture of cores and processors.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to demonstrate system on chip design models.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to hypothesize and synthesize working of advanced embedded systems.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to develop design SOC controller.</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to design, implement and test SOC model.</td>
</tr>
</tbody>
</table>

UNIT I

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSMD data-path, simulation and RTL synthesis, language mapping for FSMD.

UNIT II

Micro-programmed Architectures: limitations of FSM, Micro-programmed: control, encoding, data-path, Micro-programmed machine implementation, handling Micro-program interrupt and pipelining, General purpose embedded cores, processors, The RISC pipeline, program organization, analyzing the quality of compiled code,
**UNIT III**

System on Chip, concept, design principles, portable multimedia system, SOC modelling, hardware/software interfaces, synchronization schemes, memory mapped Interfaces , coprocessor interfaces, coprocessor control shell design, data and control design, Programmer’s model.

**UNIT IV**

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

**UNIT V**

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS

**UNIT VI**

SOC memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

**Textbooks / References:**

1. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer
**ELECTIVE-II**
**OPTICAL FIBER COMMUNICATION**

Weekly Teaching Hours  TH : 03  Tut:  --

Scheme of Marking  TH : 60  Tests : 20  IA: 20  Total : 100

**Course Objectives:**

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<tbody>
<tr>
<td><strong>A</strong></td>
<td>To expose the students to the basics of signal propagation through optical fibers, fiber impairments, components and devices and system design.</td>
</tr>
<tr>
<td><strong>B</strong></td>
<td>To provide an in-depth understanding needed to perform fiber-optic communication system engineering calculations, identify system tradeoffs, and apply this knowledge to modern fiber optic systems.</td>
</tr>
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</table>

**Course Outcomes:**

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<tbody>
<tr>
<td><strong>CO1</strong></td>
<td>Learner will be able to recognize and classify the structures of Optical fiber and types.</td>
</tr>
<tr>
<td><strong>CO2</strong></td>
<td>Learner will be able to demonstrate electromagnetic and mathematical analysis of light wave propagation.</td>
</tr>
<tr>
<td><strong>CO3</strong></td>
<td>Learner will be able to analyze fabrication techniques of different optical fibers.</td>
</tr>
<tr>
<td><strong>CO4</strong></td>
<td>Learner will be able to interpret behavior of pulse signal and various loss mechanism.</td>
</tr>
<tr>
<td><strong>CO5</strong></td>
<td>Learner will be able to interpret Dispersion compensation mechanism, Scattering effects and modulation techniques.</td>
</tr>
<tr>
<td><strong>CO6</strong></td>
<td>Learner will be able to interpret working of Fiber based devices.</td>
</tr>
</tbody>
</table>

**UNIT I**

Introduction and importance of Fiber Optics Technology, Ray analysis of optical fiber: Propagation mechanism of rays in an optical fiber, Meridional rays, Skew rays, Fiber numerical aperture, dispersion.

**UNIT II**

Electromagnetic (modal) analysis of Step index multimode fibers: Wave equation and boundary conditions, Characteristics equation, TE, TH and Hybrid modes, Weakly guiding approximation, linearly polarized modes, Single mode fiber, V parameter, Power confinement and mode cutoff, Mode field diameter.

**UNIT III**

Graded-index fiber: Modal analysis of graded index fiber, WKB analysis, Optimum profile. Experimental techniques in fiber optics: Fiber fabrication (OVD, VAD, CVD, MCVD, PMCVD etc.) and characterization, Splices, Connectors and fiber cable.
UNIT IV


UNIT V


UNIT VI


Textbooks / References:
ELECTIVE-II
STATISTICAL SIGNAL PROCESSING

Weekly Teaching Hours
TH : 03    Tut:  --

Scheme of Marking
TH : 60    Tests : 20    IA: 20    Total : 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To provide in-depth understanding of more advanced probability theory, leading into random process theory and focus on discrete time methods.</td>
</tr>
<tr>
<td>B</td>
<td>To provide in-depth understanding of fundamental concepts of statistical signal processing.</td>
</tr>
</tbody>
</table>

Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to generalize the properties of statistical models in the analysis of Signals using Stochastic processes.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to compare different Stochastic Processes and Models.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to demonstrate optimum linear filter algorithms and structures.</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to Differentiate the prominence of various spectral estimation techniques for Achieving higher resolution in the estimation of power spectral density.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to visualize Least Square Filtering and Computation techniques.</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to interpret adaptive filtering and its applications.</td>
</tr>
</tbody>
</table>

UNIT I
Introduction


UNIT II
Stochastic Processes and Models

UNIT III

Optimum Linear Filters


UNIT IV

Algorithms and Structures For Optimum Filters.


UNIT V

Least Square Filtering


UNIT VI

Adaptive Filtering


Textbooks / References:
1. Adaptive Filter Theory; S. Haykin; PHI.
ELECTIVE-II
MICROELECTRONICS

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH : 60  Tests : 20  IA: 20  Total : 100

Course Objectives:

A  To provide in-depth understanding and to be able to apply basic concepts of semiconductor physics relevant to devices

B  To be able to analyze and design microelectronic circuits for linear amplifier and digital applications

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to discuss MOS structure in terms of different parameters</th>
</tr>
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<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to express different CMOS technologies</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will get knowledge of design rules for the CMOS design</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand how devices and integrated circuits are fabricated and describe discuss modern trends in the microelectronics industry</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to determine the frequency range of simple electronic circuits and understand the high frequency limitations of BJTs and MOSFETs</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to design simple devices and circuits to meet stated operating specifications</td>
</tr>
</tbody>
</table>

UNIT I


UNIT II

CMOS Technologies: Background, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Isolation, Gate Oxide, Gate and Source/Drain Formation, Contacts and Metallization, Passivation, Metrology.

UNIT III

Layout Design Rules: Design Rules Background, Scribe Line and Other Structures, MOSIS Scalable CMOS Design Rules, Micron Design Rules. CMOS Process Enhancements:

UNIT IV

UNIT V
Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip-Flops, Circuit Families: Static CMOS, Ratioed Circuits,

UNIT VI

Textbooks / References:
COMMUNICATION SKILLS

Weekly Teaching Hours  TH: 02  Practical: -

Scheme of Marking  TH: --  IA: 25  PR/OR: 25  Total: 50

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To become more effective confident speakers and deliver persuasive presentations</td>
</tr>
<tr>
<td>B</td>
<td>To develop greater awareness and sensitivity to some important considerations in interpersonal communication and learn techniques to ensure smoother interpersonal relations</td>
</tr>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand the fundamental principles of effective business communication</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to apply the critical and creative thinking abilities necessary for effective communication in today's business world</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to organize and express ideas in writing and speaking to produce messages suitably tailored for the topic, objective, audience, communication medium and context</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to demonstrate clarity, precision, conciseness and coherence in your use of language</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to become more effective confident speakers and deliver persuasive presentations</td>
</tr>
</tbody>
</table>

UNIT I

Introduction to communication, Necessity of communication skills, Features of good communication, Speaking skills, Feedback & questioning technique, Objectivity in argument

UNIT II

Verbal and Non-verbal Communication, Use and importance of non-verbal communication while using a language, Study of different pictorial expressions of non-verbal communication and their analysis

UNIT III

Academic writing, Different types of academic writing, Writing Assignments and Research Papers, Writing dissertations and project reports

UNIT IV

Presentation Skills: Designing an effective Presentation, Contents, appearance, themes in a presentation; Tone and Language in a presentation, Role and Importance of different tools for effective presentation
UNIT V
Motivation/Inspiration: Ability to shape and direct working methods according to self-defined criteria; Ability to think for oneself, Apply oneself to a task independently with self-motivation, Motivation techniques: Motivation techniques based on needs and field situations

UNIT VI
Self-management, Self-evaluation, Self-discipline, Self-criticism, Recognition of one’s own limits and deficiencies, dependency etc. Self-awareness, Identifying one’s strengths and weaknesses, Planning & Goal setting, Managing self-emotions, ego, pride leadership & Team dynamics

TEXTBOOKS/REFERENCE:
PG LAB-I

Weekly Teaching Hours

TH: -- Practical: 03

Scheme of Marking

TH: -- IA: 25 PR/OR: 25 Total: 50

Practical’s of the Lab - I shall be based on the courses of first semester. The lab work shall consists of hands on experiments on the different software and hardware platforms related to the syllabus.
PRODUCT DESIGN & QUALITY MANAGEMENT

Weekly Teaching Hours  TH : 03   Tut: 01
Scheme of Marking    TH :60   Tests : 20   IA: 20   Total : 100

Course Objectives:

| A | To provide a foundation in product development process |
| B | To provide a foundation in Quality principles and tools |
| C | To practice in the application of product development process and quality concepts in real life scenario |

Course Outcomes:

| CO1 | Learner will be able to understand the product development process |
| CO2 | Learner will be able to apply the quality principles and tools for continuous process improvement and problem solving |
| CO3 | Learner will acquire knowledge of tools and techniques for quality management |

UNIT I


UNIT II

Product Design and Development: II Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property

UNIT III

Product Development Economics, Managing Product Development Projects.

UNIT IV


UNIT V


UNIT VI


Textbooks / References:

33
EMBEDDED OS & RTOS

Weekly Teaching Hours
TH : 03   Tut: 01

Scheme of Marking
TH :60   Tests : 20   IA: 20   Total : 100

Course Objectives:

A  To provide understanding of the techniques essential to the design and implementation of device drivers and kernel internals of embedded operating systems.

B  To provide the students with an understanding of the aspects of the Real-time systems and Real-time Operating Systems.

C  To provide an understanding of the techniques essential to the design and implementation of real-time embedded systems.

Course Outcomes:

CO1  Learner will understand the Embedded Real Time software that is needed to run embedded systems

CO2  Learner will understand the open source RTOS and their usage.

CO3  Learner will understand the VxWorks RTOS and realtime application programming with it

CO4  Learner will be able to build device driver and kernel internal for Embedded OS & RTOS

UNIT I
Embedded OS (Linux) Internals Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication – Semaphore, Pipes, FIFO.

UNIT II
Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling. Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network

UNIT III
UNIT IV
Converting a normal Linux kernel to real time kernel, Xenomai basics. Overview of Open source RTOS for Embedded systems (Free RTOS/ ChibiosRT) and application development.

UNIT V

UNIT VI
Case study Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar), Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board

Textbooks / References:
1. Venkateswaran Sreekrishnan, Essential Linux Device Drivers,
2. J. Cooperstein, Writing Linux Device Drivers: A Guide with Exercises,
5. Laplante, Phillip A, Real-Time Systems Design and Analysis : An Engineer's Handbook:
9. Simon, David E.Embedded Software Primer:
ELECTIVE-III
FPGA SYSTEM DESIGN

Weekly Teaching Hours      TH : 03     Tut: --

Scheme of Marking          TH :60     Tests : 20     IA: 20     Total : 100

Course Objectives:

A
The goal is to enable students to design and implement custom computing systems with FPGAs. Students will gain knowledge and understanding of different technologies to implement digital computing systems. Various FPGA architectures. Automated design flows supporting designs with FPGAs. Fundamentals of the FPGA design tools. The reconfigurable computing systems and the roles of FPGAs in those systems.

Course outcomes

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to Translate a software application into hardware logic for FPGA architectures</th>
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<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to Design synthesizable VHDL systems based on industry-standard coding methods.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to Optimize logic for various performance goals (timing, frequency, area, and power).</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to Simulate and compare performance results between different optimizations.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to Utilize commercial FPGA development tools for compilation, simulation, and synthesis.</td>
</tr>
</tbody>
</table>

UNIT I
Introduction to Asics, CMOS Logic and ASIC Library Design
Types of ASICs - Design Flow - CMOS transistors, CMOS design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - transistors as resistors - transistor parasitic capacitance - Logical effort - Library cell design - Library architecture

UNIT II
Programmable Logic Cells and I/O Cells
Digital clock Managers-Clock management- Regional clocks- Block RAM – Distributed RAM Configurable Logic Blocks-LUT based structures – Phase locked loops- Select I/O resources –Anti fuse - static RAM - EPROM and EEPROM technology.

UNIT III
Device Architectures
Device Architecture-Spartan 6 -Vertex 4 architecture- Altera Cyclone and Quartus architectures
UNIT IV
Design Entry and Testing

UNIT V
Floor Planning, Placement And Routing System partition - FPGA partitioning - partitioning methods - floor planning - placement

UNIT VI
Physical design flow - global routing - detailed routing - special routing - circuit extraction – DRC

Textbooks / References:
3. Design manuals of Altera, Xilinx and Actel.
Elective-III
WIRELESS SENSOR NETWORK DESIGN

Weekly Teaching Hours  TH : 03  Tut: --
Scheme of Marking  TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>To provide in-depth understanding of design and implementation of WSN</td>
</tr>
<tr>
<td>B</td>
<td>To provide ability to formulate and solve problems creatively in the area of WSN</td>
</tr>
<tr>
<td>C</td>
<td>To provide in-depth understanding of various applications of WSN.</td>
</tr>
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Course Outcomes:

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<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand the need of WSN and also will analyze the challenges in creating WSN</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to design the architecture of WSN</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to analyze the power and security constraints in WSN</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand different operating system to operate WSN</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand the basic functioning of WSN at physical layer</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to understand different protocols at network layer to for multiple channel accessing</td>
</tr>
</tbody>
</table>

UNIT I


UNIT II

Architectures: Node Architecture, the sensing subsystem, processor subsystem, communication, interface, LMote, XYZ, Hogthrob node architectures

UNIT III


UNIT IV

UNIT V

Physical Layer – Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation

UNIT VI

Medium Access Control – types, protocols, standards and characteristics, challenges, Network Layer - Routing Metrics, different routing techniques.

Textbooks / References:
ELECTIVE-III
VLSI AND MICROSYSTEMS

Weekly Teaching Hours  
TH : 03  
Tut:  --  

Scheme of Marking  
TH :60  
Tests : 20  
IA: 20  
Total : 100

Course Objectives:

A  
To provide in depth understanding of the principals involved in the latest hardware required for designing and critically analyzing electronic circuits relevant to industry need and society

B  
To provide in depth understanding of micro fabrication process, packaging

Course Outcomes:

| CO1 | Learner will be able to understand the different abstract levels in Verilog for modeling Digital circuits. |
| CO2 | Learner will be able to understand the designing of combinational and sequential circuits in CMOS |
| CO3 | Learner will be able to understand CMOS analog circuits design |
| CO4 | Learner will be able to understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits |
| CO5 | Learner will be able to understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers |
| CO6 | Learner will be able to understand implementation of finite element method for different semiconductor devices |

UNIT I

VHDL Modeling and PLD Architectures

UNIT II

SoC, Interconnect and Digital CMOS Circuits

Clock skew, Clock distribution techniques, clock jitter. Supply and ground bounce, power distribution techniques. Power optimization. Interconnect routing techniques; wire parasitic, Signal integrity issues. I/O architecture, pad design, Architectures for low power, MOS Capacitor, MOS Transistor theory, C-V characteristics, Non ideal I-V effects, Technology Scaling. CMOS inverters, DC transfer characteristics, Power components, Power delay product. Transmission gate. CMOS combo logic design. Delays: RC delay model, Effective resistance, Gate and diffusion capacitance, Equivalent RC circuits; Linear delay model, Logical effort, Parasitic delay, Delay in a logic gate, Path logical efforts.

UNIT III

Analog CMOS Design and Testability


UNIT IV

Microfabrication processes

Glimpses of Microsystems, scaling effects, Smart materials and systems: an overview, Microsensors: some examples, Microactuators: some examples, Microsystems: some examples, Examples of smart systems: structural health monitoring and vibration control, Structure of silicon and other materials, Silicon wafer processing; Thin-film deposition, Lithography, wet etching and dry etching Bulk micromachining and Surface micromachining, Wafer-bonding; LIGA and other moulding techniques, Soft lithography and polymer processing, Thick-film processing; Low temperature co-fired ceramic Processing, Smart material processing.

UNIT V

Mechanics of Solids

Stresses and deformation: bars and beams, Micro device suspensions: lumped modeling, Residual stress and stress gradients, Poisson effect; Anticlastic curvature; examples of micromechanical structures, Thermal loading; bimorph effect, Dealing with large displacements; in-plane and 3D elasticity equations, Vibrations of bars and beams, Gyroscopic effect, Frequency response; damping; quality factor, Basic micro-flows for damping calculation.
UNIT VI

Finite element method and Electronics and packaging

Types of numerical methods for solving partial differential equations, finite element method, Variational principles, Weak form; shape functions, Isoparametric formulation and numerical integration, Implementation of the finite element method, FEM for piezoelectrics, Semiconductor devices: basics, OpAms and OpAmp circuits, Signal conditioning for microsystems devices, Control and microsystems, Vibration control of a beam, Integration of microsystems and microelectronics, Packaging of Microsystems: why and how, Flip-chip, ballgrid, etc., reliability, Case-study 1 (Pressure sensor), Case-study 2 (Accelerometer)

Textbooks / References:

ELECTIVE III
INFORMATION SECURITY

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

A. To provide students with concepts of computer security, cryptography, digital money, secure protocols, detection and other security techniques.

Course Outcomes:

<table>
<thead>
<tr>
<th>CO</th>
<th>Course Outcome</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will acquire knowledge of various data hiding techniques</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able identify malicious/harmful programs and concept of firewall</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to express OSI layer and protocols and IP security</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to interpret authentication applications</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to relate security protocols to wireless networks</td>
</tr>
</tbody>
</table>

UNIT I

UNIT II

UNIT III

UNIT IV

UNIT V

Textbooks / References:

1. William Stallings Cryptography and Network Security: Principles and Practice-
2. Timothy Stapko, Publisher Newnes. Practical Embedded Security: Building Secure Resource Constrained Systems -
4. Information Security for Technical Staff-SEI.
5. Guide to firewalls & network security: with intrusion detection & VPNs- HOLDEN, GREG.
**ELECTIVE IV**

**ASIC AND SOC**

<table>
<thead>
<tr>
<th>Weekly Teaching Hours</th>
<th>TH : 03</th>
<th>Tut: --</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme of Marking</td>
<td>TH :60</td>
<td>Tests : 20</td>
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**Course Objectives:**

<p>| | |</p>
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<tr>
<th></th>
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<tbody>
<tr>
<td>A</td>
<td>To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.</td>
</tr>
<tr>
<td>B</td>
<td>To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.</td>
</tr>
<tr>
<td>C</td>
<td>To give the student an understanding of basics of System on Chip and Platform based design.</td>
</tr>
</tbody>
</table>

**Course Outcomes:**

| CO1 | Learner will be able to demonstrate VLSI tool-flow and appreciate FPGA architecture. |
| CO2 | Learner will be able to understand the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design. |
| CO3 | Learner will be able to understand the algorithms used for ASIC construction |
| CO4 | Learner will be able to understand the basics of System on Chip |
| CO5 | Learner will be able to tackle system level design issues |

**Unit I**

**Types of ASICs** – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

**Unit II**

**ASIC Library design:** Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC, ASIC Construction – Floor planning & placement – Routing

**Unit III**

**System on Chip Design Process:** A canonical SoC design, SoC Design Flow – Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process,

**Unit IV**

**System level design issues**- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues;
Unit V
Verification Strategy On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies. MPSoCs. Techniques for designing MPSoCs

Unit VI
SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.

Textbooks / References:
ELECTIVE-IV
RECONFIGURABLE COMPUTING

Weekly Teaching Hours
TH : 03   Tut: --

Scheme of Marking
TH :60   Tests : 20   IA: 20   Total : 100

Course Objectives:

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td>A</td>
<td>To learn the basics of field of reconfigurable computing</td>
</tr>
<tr>
<td>B</td>
<td>To learn Advance digital design skills by developing a reconfigurable computing application  Learn a hardware design language Chisel - An introduction to research methodology</td>
</tr>
</tbody>
</table>

Course Outcomes:

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand concept of static and dynamic reconfiguration.</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to use the basics of the PLDs for designing reconfigurable circuits.</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to understand the reconfigurable system design using HDL</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to demonstrate different architectures of reconfigurable computing.</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand different applications of reconfigurable computing</td>
</tr>
</tbody>
</table>

UNIT I

Types of computing and introduction to RC: General Purpose Computing, Domain-Specific Processors, Application Specific Processors; Reconfigurable Computing, Fields of Application; Reconfigurable Device Characteristics, Configurable, Programmable, and Fixed-Function Devices; General-Purpose Computing, General-Purpose Computing Issues;

UNIT II

Metrics: Density, Diversity, and Capacity; Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement

UNIT III

Routing; Computing Elements, LUTs, LUT Mapping, ALU and CLBs; Retiming, Fine-grained & Coarse-grained structures; Multi-context;

UNIT IV

Different architectures for fast computing viz. PDSPs, RALU, VLIW, Vector Processors, Memories, CPLDs, FPGAs, Multi-context FPGA, Partial Reconfigurable Devices; Structure
and Composition of Reconfigurable Computing Devices: Interconnect, Instructions, Contexts, Context switching, RP space model;

**UNIT V**

Reconfigurable devices for Rapid prototyping, Non-frequently reconfigurable systems, Frequently reconfigurable systems; Compile-time reconfiguration, Run-time reconfiguration

**UNIT VI**

Architectures for Reconfigurable computing: TSFPGA, DPGA, Matrix; Applications of reconfigurable computing: Various hardware implementations of Pattern Matching such as the Sliding Windows Approach, Automaton-Based Text Searching, Video Streaming

**Textbooks / References:**

1. Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”.
2. IEEE Journal papers on Reconfigurable Architectures.
ELECTIVE-IV
ELECTRONIC PACKAGING

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

<table>
<thead>
<tr>
<th>Course</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>To sensitize the undergraduate students and graduate students to the all-important multidisciplinary area of electronics systems packaging.</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to describe the functions and applications of packages and materials used for packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to explain the procedure used for evaluating the electrical aspects of packaging</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to describe component of CAD packages</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to explain the technique used for fabrication and characteristics of single layer and multi-layer PCBs and compare their performances</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to describe about thermal management techniques for packages and reliability of packages</td>
</tr>
</tbody>
</table>

UNIT I
Overview of electronic systems packaging, Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications, Definition of PWB. Video on “Sand-to-Silicon”, Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flipchip-1, Wire bonding, TAB and flipchip-2.

UNIT II
Necessary of packaging. Types, Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging, Multichip modules (MCM)-types; Systeminpackage (SIP); Packaging roadmaps; Hybrid circuits; Electrical Issues – I; Resistive Parasitic, Electrical Issues – II; Capacitive and Inductive Parasitic, Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.

UNIT III
Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights, Design Flow considerations; Beginning a circuit design with schematic work and component layout, Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for
Reliability. Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued

**UNIT IV**

Video highlights; Surface preparation, Photoresist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; Resist stripping; Screenprinting technology, Through-hole manufacture process steps; Panel and pattern plating methods. Video highlights on manufacturing; Solder mask for PWBs; Multilayer PWBs; Introduction to microvias, Microvia technology and Sequential build-up technology process flow for high-density interconnects, Conventional Vs HDI technologies; Flexible circuits; Tutorial session.

**UNIT V**

SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave soldering, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues.

**UNIT VI**

Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.

**Textbooks / References:**

ELECTIVE IV
ROBOTICS AND MACHINE VISION

Weekly Teaching Hours | TH : 03 | Tut: --
Scheme of Marking | TH :60 | Tests : 20 | IA: 20 | Total : 100

Course Objectives

<p>| | |</p>
<table>
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<tr>
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<tbody>
<tr>
<td>A</td>
<td>To familiarize students with the concepts and techniques of robot manipulator, its kinematics, programming and build confidence to evaluate, choose and incorporate robots in engineering systems.</td>
</tr>
</tbody>
</table>

Course Outcome:

| CO1 | Learner will be able to express basic concept of robotics |
| CO2 | Learner will be able to locate industrial applications of robots |
| CO3 | Learner will be able to distinguish between human vision and machine vision |
| CO4 | Learner will be able to perform image processing techniques and transformation |
| CO5 | Learner will be able to perform image analysis |

UNIT I
Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations

UNIT II
Industrial Applications of Robots, and Programming

UNIT III

UNIT IV

UNIT V
UNIT VI

**Edge Enhancement Techniques and Image Analysis:** Introduction, Digital Filters – Low pass and High Pass filters; Edge Enhancement Operators – Laplacian, Roberts Gradient, Sobel and other Local operators. Image Analysis: Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm.

**Textbooks / References:**

7. Sonka, Milan Et Al, *Image Processing, Analysis And Machine Vision*
ELECTIVE V
INTERNET OF THINGS

Weekly Teaching Hours
TH : 03   Tut: --

Scheme of Marking
TH :60 Tests : 20 IA: 20 Total : 100

Course Objectives:

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<tbody>
<tr>
<td>A</td>
<td>Students will be explored to the interconnection and integration of the physical world and the cyber space.</td>
</tr>
<tr>
<td>B</td>
<td>To provide ability to design and develop IOT devices.</td>
</tr>
</tbody>
</table>

Course Outcomes:

| CO1 | Learner will be able to understand the meaning of internet in general and IOT in terms of layers, protocols, packets peer to peer communication |
| CO2 | Learner will be able to interpret IOT working at transport layer with the help of various protocols |
| CO3 | Learner will be able to understand IOT concept at data link layer |
| CO4 | Learner will be able to apply the concept of mobile networking to the internet connected devices |
| CO5 | Learner will be able to measure and schedule the performance of networked devices in IOT |
| CO6 | Learner will be able to analyze the challenges involve in developing IOT architecture |

UNIT I
Introduction: What is the Internet of Things: History of IoT, about objects/things in the IoT, Overview and motivations, Examples of applications, IoT definitions, IoT Frame work, General observations, ITU-T views, working definitions, and basic nodal capabilities.

UNIT II
Fundamental IoT Mechanisms & Key Technologies : Identification of IoT objects and services, Structural aspects of the IoT, Environment characteristics, Traffic characteristics, scalability, Interoperability, Security and Privacy, Open architecture, Key IoT Technologies, Device Intelligence, Communication capabilities, Mobility support, Device Power, Sensor Technology, RFID technology, Satellite Technology.

UNIT III

UNIT IV
Wireless Technologies For IoT : Layer ½ Connectivity : WPAN Technologies for IoT/M2M, Zigbee /IEEE 802.15.4, Radio Frequency for consumer Electronics ( RF4CE), Bluetooth and
its low-energy profile, IEEE 802.15.6 WBANS, IEEE 802.15 WPAN TG4j, MBANS, NFC, dedicated short range communication (DSRC) & related protocols. Comparison of WPAN technologies cellular & mobile network technologies for IoT/M2M.

UNIT V


UNIT VI

Internet of Things Application Examples: Smart Metering, advanced metering infrastructure, e-Health/Body area network, City automation, automotive applications. Home automation, smart cards, Tracking, Over-The-Air passive surveillance/Ring of steel, Control application examples.

Textbooks / References:

2. Daniel Minoli, Building the Internet of Things with IPv6 and MIPv6 The Evolving World of M2M Communications, Wiley Publications
ELECTIVE V
LINEAR ALGEBRA

Weekly Teaching Hours
TH : 03    Tut: --

Scheme of Marking
TH :60    Tests : 20    IA: 20    Total : 100

Course Objectives:

<table>
<thead>
<tr>
<th></th>
<th>To provide in-depth understanding of fundamental concepts of linear algebra</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>To understand the importance of linear algebra and learn its applicability to practical problems</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Student will learn to solve and analyze linear system of equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Student will analyze the direct notations, duality, adjointness, bases, dual bases in linear algebra</td>
</tr>
<tr>
<td>CO3</td>
<td>Student will understand the concept of Linear transformations and matrices, equivalence, similarity.</td>
</tr>
<tr>
<td>CO4</td>
<td>Student will be able to find eigen values and eigen vectors using characteristics polynomials</td>
</tr>
<tr>
<td>CO5</td>
<td>Student will learn to find the singular value decomposition of the matrix</td>
</tr>
<tr>
<td>CO6</td>
<td>Student will be to find the inverse of matrix</td>
</tr>
</tbody>
</table>

UNIT I
Fields Fq, R, C. Vector Spaces over a field, Fn, F[œ]=Polynomials in one Variable.

UNIT II
Direct Notations, Ket, bra vector, duality, adjointness, linear transformations, bases, dual bases.

UNIT III
Linear transformations and matrices, equivalence, similarity.

UNIT IV
Eigenvalues, eigenvectors, diagonalization, Jordancanonical form

UNIT V
Bilinear and sesquilinear forms, inner product, orthonormal, bases, orthogonal decomposition, projections

UNIT VI
System of equations, generalized inverses.
Textbooks / References:
ELECTIVE V
NEURAL NETWORKS IN EMBEDDED APPLICATIONS

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

<table>
<thead>
<tr>
<th></th>
<th>To be able to use analogy of human neural network for understanding of artificial learning algorithms.</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>To give in-depth understanding of fundamental concepts of neural network</td>
</tr>
<tr>
<td>C</td>
<td>To exhibit the knowledge of radial basis function network</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th></th>
<th>Learner will be able to understand concept of fuzzy logic.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO1</td>
<td>Learner will be able to understand embedded digital signal processor, Embedded system design and development cycle, applications in digital camera</td>
</tr>
<tr>
<td>CO2</td>
<td>Learner will be able to understand embedded systems, characteristics, features and applications of an embedded system</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to design and utilization of fuzzy logic controller for various industrial applications</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to implement of radial basis function, neural network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine</td>
</tr>
</tbody>
</table>

UNIT I
Introduction to artificial neural networks, Fundamental models of artificial neural network, Perceptron networks, feed forward networks, Feedback networks, Radial basis function networks, Associative memory networks

UNIT II

UNIT III
UNIT IV
Introduction to Embedded systems, Characteristics, Features and Applications of an embedded system

UNIT V
Introduction to embedded digital signal processor, Embedded system design and development cycle, ANN application in digital camera,

UNIT VI
Implementation of Radial Basis Function, Neural Network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

Textbooks / References:
2. Simon Haykin, “Neural Networks: Comprehensive foundation”, Prentice Hall Publication
ELECTIVE V
RESEARCH METHODOLOGY

Weekly Teaching Hours  TH : 03  Tut:  --
Scheme of Marking    TH :60  Tests : 20  IA: 20  Total : 100

**Course Objectives:**

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<tbody>
<tr>
<td>A</td>
<td>To develop a research orientation among the scholars and to acquaint them with fundamentals of research methods.</td>
</tr>
<tr>
<td>B</td>
<td>To develop understanding of the basic framework of research process.</td>
</tr>
<tr>
<td>C</td>
<td>To identify various sources of information for literature review and data collection.</td>
</tr>
<tr>
<td>D</td>
<td>To understand the components of scholarly writing and evaluate its quality.</td>
</tr>
</tbody>
</table>

**Course Outcomes:**

| CO1 | Student will learn the meaning, objective, motivation and type of research |
| CO2 | Student will be able to formulate their research work with the help of literature review |
| CO3 | Student will be able to develop an understanding of various research design and techniques |
| CO4 | Student will have an overview knowledge of modeling and simulation of research work |
| CO5 | Student will be able to collect the statistical data with different methods related to research work |
| CO6 | Student will be able to write their own research work with ethics and non-plagiarized way |

**UNIT I**
Introduction: Defining research, Motivation and Course Objective:s, Types of research
Meaning of Research, Course Objective:s of Research, Motivation in Research, Types of Research

**UNIT II**
Research Formulation: Formulating The research Problem, Literature Review, Development of Working Hypothesis

**UNIT III**

**UNIT IV**
Overview of Modeling and Simulation: Classification of models, Development of Models, Experimentation, Simulation.
UNIT V
Statistical Aspects: Methods of Data Collection, Sampling Methods, Statistical analysis, Hypothesis testing.

UNIT VI

Textbooks / References:
1. J.P. Holman, Experimental Methods for Engineers
2. C.R. Kothari, Research Methodology, Methods & Techniques
ELECTIVE V
WAVELET TRANSFORMS AND ITS APPLICATIONS

Weekly Teaching Hours
TH : 03  Tut: --

Scheme of Marking
TH :60  Tests : 20  IA: 20  Total : 100

Course Objectives:

<table>
<thead>
<tr>
<th></th>
<th>To provide in-depth understanding of fundamental concepts of Wavelets.</th>
</tr>
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<tbody>
<tr>
<td>B</td>
<td>To study wavelet related constructions, its applications in signal processing, communication and sensing.</td>
</tr>
</tbody>
</table>

Course Outcomes:

<table>
<thead>
<tr>
<th>CO1</th>
<th>Learner will be able to understand the meaning of wavelet transform</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO2</td>
<td>Learner will be able to understand the terminologies used in Wavelet transform with its properties</td>
</tr>
<tr>
<td>CO3</td>
<td>Learner will be able to demonstrate various filter bank using wavelet transformation</td>
</tr>
<tr>
<td>CO4</td>
<td>Learner will be able to understand bases, orthogonal bases in wavelet transform</td>
</tr>
<tr>
<td>CO5</td>
<td>Learner will be able to understand different types of wavelet transform</td>
</tr>
<tr>
<td>CO6</td>
<td>Learner will be able to design practical system using wavelet transform</td>
</tr>
</tbody>
</table>

UNIT I
Continuous Wavelet Transform Introduction, Continuous-time wavelets, Definition of the CWT, the VWT as a Correlation, Constant-Factor Filtering Interpretation and Time-Frequency Resolution, the VWT as an Operator, Inverse CWT, Problems.

UNIT II
Introduction to Discrete Wavelet Transform And Orthogonal Wavelet Decomposition: Introduction, Approximation of Vectors in Nested Linear Vector Subspaces, Examples of an MRA, Problems.

UNIT III
MRA, Orthonormal Wavelets, And Their Relationship To Filter Banks: Introduction, Formal Definition of an MRA, Construction of General Orthonormal MRA, a wavelet Basic for the MRA,

UNIT IV
Digital Filtering Interpretation, Examples of Orthogonal Basic Generating Wavelets, Interpreting Orthonormal MRAs for Discrete-Time signals, Miscellaneous Issues Related to
PRQME Filter Banks, generating Scaling Functions and wavelets from Filter Coefficient, Problems.

UNIT V
Wavelet Transform And Data Compression: Introduction, Transform Coding, DTWT for Image Compression, Audio Compression, And Video Coding Using Multiresolution Techniques: a Brief Introduction.

UNIT VI

Textbooks / References:
1. C. Sidney Burrus, R. A. Gopianath, Pretice Hall, Introduction to Wavelet and Wavelet Transform
2. P.P.Vaidyanathan , PTR Prentice Hall, Englewood Cliffs , New Jersey, Multirate System and Filter Banks
4. Raghuveer Rao, Ajit Bopardikar, Pearson Education Asia,Wavelet Transforms Introduction to Theory and Application
SEMINAR I

Weekly Teaching Hours  TH: -  Practical:  04
Scheme of Marking  IA: 50  PR/OR: 50  Total: 100

The seminar shall be on the state of the art in the area of the wireless communication and computing and of student’s choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute.
The mini project shall be based on the recent trends in the industry, research and open problems from the industry and society. This may include mathematical analysis, modelling, simulation, and hardware implementation of the problem identified. The mini project shall be of the student’s choice and approved by the guide. The student has to submit the report of the work carried out in the prescribed format signed by the guide and head of the department/institute.
PROJECT MANAGEMENT AND INTELLECTUAL PROPERTY RIGHTS

Weekly Teaching Hours TH: - Practical: -
Scheme of Marking IA: 50 PR/OR: 50 Total: 100

The Student has to choose this course either from NPTEL/MOOCs/SWAYAM pool. It is mandatory to get the certification of the prescribed course.
PROJECT-I

Weekly Teaching Hours  TH: -  Practical: -

Scheme of Marking  IA: 50  PR/OR: 50  Total: 100

Project-I is an integral part of the final project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation that may include mathematical model/SRS/UMl/ERD/block diagram/ PERT chart, and layout and design of the proposed system/work. As a part of the progress report of project-I work, the candidate shall deliver a presentation on progress of the work on the selected dissertation topic. It is desired to publish the paper on the state of the art on the chosen topic in international conference/journal. The student shall submit the duly certified progress report of project-I in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.
PROJECT-II

Weekly Teaching Hours

| TH: - | Practical: - |

Scheme of Marking

| IA: 100 | PR/OR: 100 | Total: 200 |

In Project - II, the student shall complete the remaining part of the project which will consist of the simulation/ analysis/ synthesis/ implementation / fabrication of the proposed project work, work station, conducting experiments and taking results, analysis and validation of results and drawing conclusions.

It is mandatory to publish the paper on the state of the art on the chosen topic in international conference/ journal.

The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the department/institute.