DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,
LONERE – RAIGAD -402 103
Mid Semester Examination – October - 2017

Branch: M.Tech. (Electronics Engineering) **Sem.:- I**

Subject with Subject Code:- VLSI System Design (MTEEC103)

Marks: 20

Date:- **Time:- 1 Hr.**

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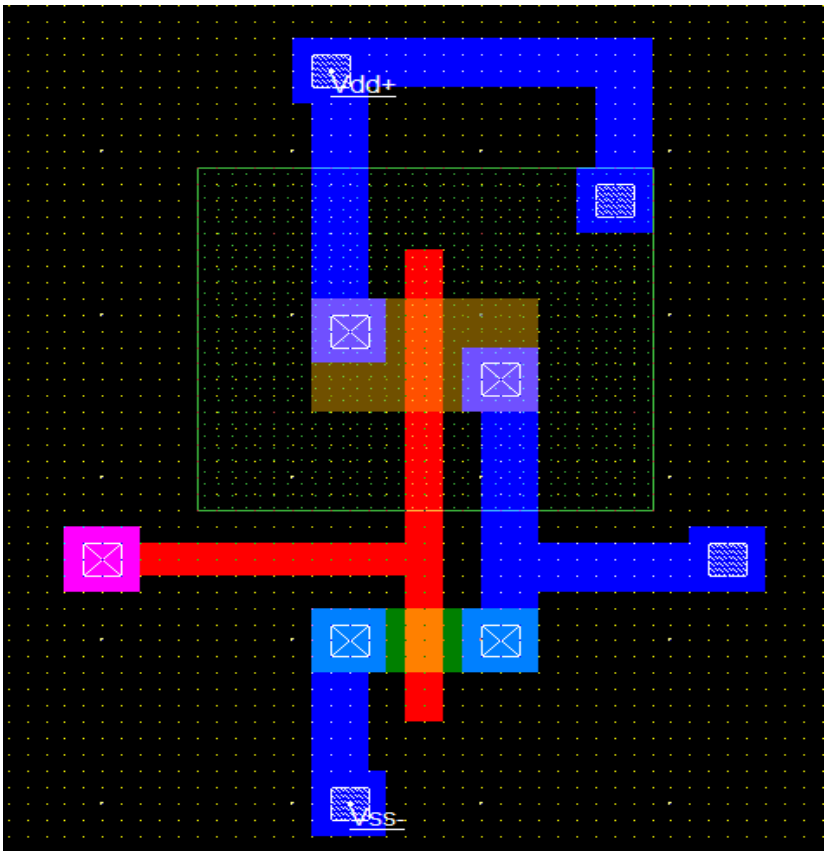
Instructions:- **Assume suitable data**

(Marks)

Q.No.1 **Attempt any one of the following** **(08)**

a) Design layout of CMOS Inverter and explain the layout design rule.

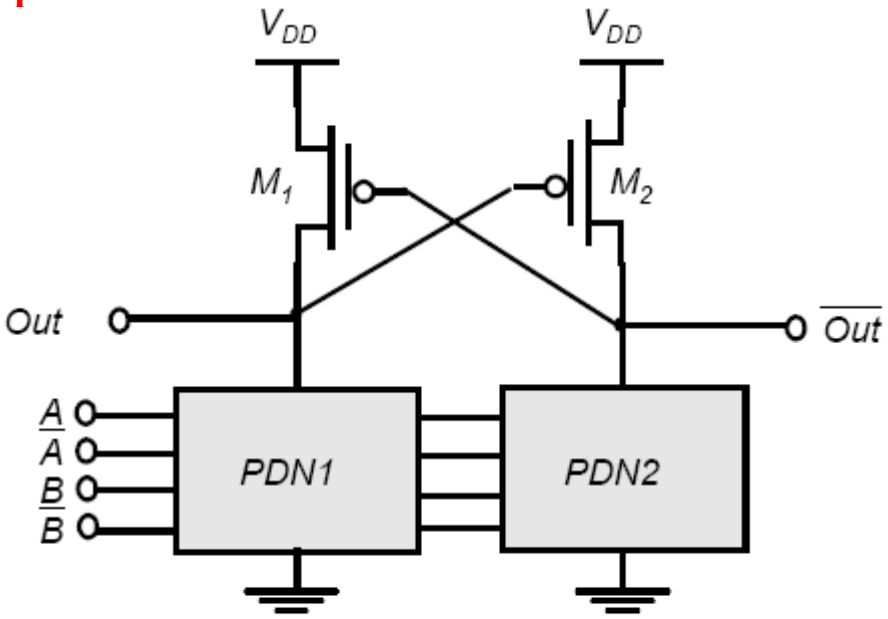
ANS:



Design rule: Write color scheme and sizes of layer
Refer Example2.5, page 87 , Author:Wayne Wolf, Title: Modern VLSI Design ,system on chip design.

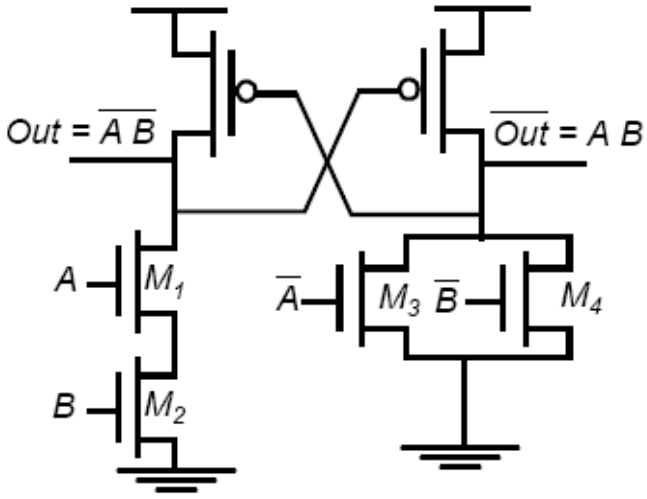
b) What is structure of a Differential cascade Voltage switch logic (DCVSL)? Explain it and draw a schematic for two input AND/NAND gates in DCVSL.

ANS: Basic Principle of DCVSL



(a) Basic principle

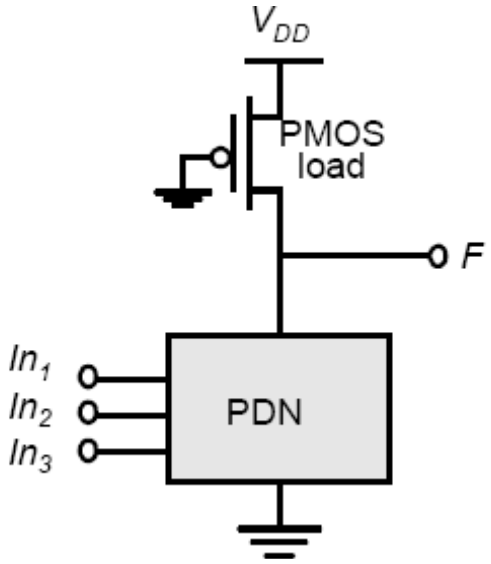
Refer -3.5.2 –DCVS Logic and Figure 3-29, page 147 ,148
Author:Wayne Wolf, Title: ModernVLSI Design ,system on chip design.



Q.No. 2 Attempt any three of the following: (12)

a) What is mean by Pseudo NMOS Logic? Why use a Pseudo-NMOS Logic?

ANS:



Refer -3.5.1 page 145 , Author:Wayne Wolf, Title: Modern VLSI Design ,system on chip design.

Or

Refer 2.5.4, Page 64, Author: Neil Weste, Title : CMOS VLSI Design

b) Assuming that Vgs=3.3v, k'=73μA/v², Compute the drain current through n-type transistors of the size W/L=5/2 at Vds value of 2V.

ANS: Refer Example2.2, page 48 , Author:Wayne Wolf, Title: Modern VLSI Design ,system on chip design.

c) Define Noise margin. Explain low noise and high noise margin with Transfer characteristics of CMOS Inverter.

ANS: Refer 2.5.3, Page 62, Author: Neil Weste, Title : CMOS VLSI Design

Or Refer -3.3.3 page 121 , Author:Wayne Wolf, Title: Modern VLSI Design ,system on chip design.

d) Describe following terms:

i) Wire and Vias

ii) Wire Parasitics

ANS: Refer:2.4, 2.4.1, page 62,65 , Author:Wayne Wolf, Title: Modern VLSI Design, system on chip design.